DOCTORAL THESIS

Common-Ground Energy Router Structure with Enhanced Reliability and Protection

Saeed Rahimpour

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation, and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

Saeed Rahimpour

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TALLINNA TEHNIKAÜLIKOOL
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Ühise nulljuhtmega suurendatud töökindluse ja kaitsega energiaruuter

SAEED RAHIMPOUR

TAL TECH
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Contents

List of publications

The list of author's publications, on the basis of which the thesis has been prepared:

[PAPER-I] S. Rahimpour, O. Husev and D. Vinnikov, "A Family of Bidirectional Solid-State Circuit Breakers with Increased Safety in DC Microgrids," in IEEE Transactions on Industrial Electronics, doi: 10.1109/TIE.2023.3337493.

[PAPER-II] S. Rahimpour, O. Husev, D. Vinnikov, N. V. Kurdkandi and H. Tarzamni, "Fault Management Techniques to Enhance the Reliability of Power Electronic Converters: An Overview," in IEEE Access, vol. 11, pp. 13432-13446, 2023.

[PAPER-III] S. Rahimpour, H. Tarzamni, N. V. Kurdkandi, O. Husev, D. Vinnikov and F. Tahami, "An Overview of Lifetime Management of Power Electronic Converters," in IEEE Access, vol. 10, pp. 109688-109711, 2022.

[PAPER-IV] S. Rahimpour, O. Husev, and D. Vinnikov, "Design and Analysis of a DC Solid-State Circuit Breaker for Residential Energy Router Application," Energies, vol. 15, no. 24, p. 9434, Dec. 2022.

[PAPER-V] S. Rahimpour, O. Husev and D. Vinnikov, "Impedance-Source DC Solid-State Circuit Breakers: An Overview," 2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Sorrento, Italy, 2022, pp. 186-191.

[PAPER-VI] T. Hemmati Shahsavar, S. Rahimpour, N. Vosoughi Kurdkandi, A. Fesenko, O. Matiushkin, O. Husev, D. Vinnikov "Comparative Evaluation of Common-Ground Converters for Dual-Purpose Application," Energies, vol. 16, no. 7, p. 2977, Mar. 2023.

[PAPER-VII] M. R. Azizi, S. Rahimpour, O. Husev, and O. Veligorskyi, "Back-to-Back Energy Router Based on Common-Ground Inverters," CPE-POWERENG 2023 – International Conference on Compatibility, Power Electronics and Power Engineering, Tallinn, Estonia, 2023.

[PAPER-VIII] N. V. Kurdkandi, O. Husev, S. Rahimpour, C. Roncero-Clemente, O. Matiushkin and D. Vinnikov, "A Novel Flying Inductor based Grid-Connected Inverter with Buck-Boost Ability," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968954.

[PAPER-IX] S. Rahimpour, O. Matiushkin, N. V. Kurdkandi, M. Najafzadeh, O. Husev and D. Vinnikov, "Model Predictive Control of a Single-Stage Flying Inductor Based Buck-Boost Grid-Connected Common-Ground Inverter," 2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 2021, pp. 1-6.

Author's contribution to the publications

Contribution to the papers in this thesis are:

[PAPER-I] Saeed Rahimpour is the main author of the paper. He proposed and simulated the circuit, calculated the parameters of the circuit, designed the PCB, and prototyped and tested the circuit.

[PAPER-II] Saeed Rahimpour as the main author of the paper, reviewed and investigated the references and authored the paper.

[PAPER-III] Saeed Rahimpour as the main author of the paper, reviewed and investigated the references and authored the paper.

[PAPER-IV] Saeed Rahimpour as the main author of the paper, proposed and simulated the circuit, calculated the parameters of the circuit, designed the PCB, and prototyped and tested the circuit.

[PAPER-V] Saeed Rahimpour as the main author of the paper, reviewed and investigated the references and authored the paper. He presented the paper at 2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM).

[PAPER-VI] Saeed Rahimpour as the co-author of the paper, reviewed and investigated the references and authored the paper.

[PAPER-VII] Saeed Rahimpour as the co-author of the paper, was responsible for methodology, surveying, writing and draft preparation.

[PAPER-VIII] Saeed Rahimpour as the co-author of the paper, was responsible for methodology, surveying, writing and draft preparation.

[PAPER-IX] Saeed Rahimpour as the main author of the paper, implemented the control technique and simulated the circuit. He calculated the parameters of the circuit and authored the paper. He presented the paper at 2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON).

Abbreviations

AC (ac)	Alternating Current
ALT	Accelerated Life Testing
ANPC	Active Neutral Point Clamped
CB	Circuit Breaker
CDF	Cumulative Distribution Function
CMC	Cascaded Multilevel Converter
SiC	Silicon Carbide
DC (dc)	Direct Current
DfR	Design for Reliability
EMI	Electromagnetic Interference
EV	Electric Vehicle
FMEA	Failure Mode and Effects Analysis
FTA	Fault-Tree Analysis
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
MC	Markov Chain
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NPS	Neutral Phase Shift
PCB	Printed Circuit Board
PDF	Probability Density Function
PV	Photovoltaic
PWM	Pulse Width Modulation
RBD	Reliability Block Diagram
RMS	Root Mean Square
RUL	Remaining Useful Life
SiC	Silicon Carbide
SSCB	Solid State Circuit Breaker
TalTech	Tallinn University of Technology
THD	Total Harmonic Distortion
TRL	Technology Readiness Level
TSV	Total Standing Voltage

Symbols

μ_V	Voltage utilization rate of the switch
V_{dc}	Input dc Voltage
P	Rated Power
V_{in}	Input Voltage
i_N	Nominal current
S_{i}	MOSFET
D_{i}	Diode
R_S	Snubber Resistor
C_S	Snubber Capacitor
MOV	Snubber MOV
L_{Line}	Input side Inductor
L_{Out}	Output side Inductor
R_{Load}	Load Resistor
R_{i}	Resistor
V_{clamp}	Maximum clamp dc voltage of MOV
E_r	Surge energy on the MOV
I_{Surge}	Maximum surge current of MOV
I_P	Peak short circuit current
v_C	Voltage of capacitor
v_{MOV}	Voltage of MOV
$R_{ds(on)}$	Drain-source on resistance of switch
K_{i}	Relay
D	Duty cycle
i_L	Current of inductor
I_{Limit}	Detection current limit
V_{GS}	Gate-source voltage
$V_{O,max}$	Maximum output voltage
AD	Damage accumulation
λ	Failure rate
π_T	Temperature Factor
π_E	Quality Factor
π_Q	Environment factor
π_J	Junction Temperature
π_S	Voltage stress factor
π_R	Current factor
N	number of power cycles generated by the rainflow counting algorithm
μ_{SSCB}	Efficiency of circuit breaker
$V_{S,max}$	Maximum voltage of the switch

1 Introduction

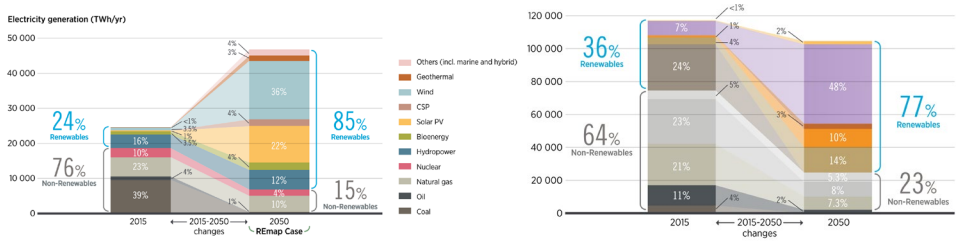
This thesis explores the development of an energy router capable of managing both ac and dc inputs efficiently. This research aims to enhance the reliability and protection mechanisms of energy routers, contributing to a sustainable and efficient energy future.

1.1 Background

The global energy landscape is undergoing a profound transformation marked by an undeniable shift towards sustainable and renewable energy sources [1]. Over the past few decades, there has been a significant increase in the generation of electricity, driven not only by escalating global energy demands but also by a growing awareness of the environmental impact of traditional non-renewable energy sources. This paradigm shift is evident in the increasing prominence of renewable energy technologies, which are gradually overtaking their non-renewable counterparts. Renewable energy technologies, including solar, wind, hydro, and geothermal, have gained momentum as viable alternatives to conventional fossil fuels and nuclear power. These sources are characterized by their inherent sustainability, lower environmental impact, and a reduced carbon footprint compared to traditional non-renewable energy sources. As demonstrated in Fig. 1.1, projections suggest that by 2050, the share of electricity generated from renewable sources will experience a remarkable upswing (from 24% to 85%), marking a transformative departure from the dominance of fossil fuels.

The rising demand for cleaner and sustainable energy sources has led to the proliferation of renewable energy systems, such as solar photovoltaics and wind turbines, which often generate dc power. Simultaneously, traditional power grids predominantly operate on ac. Most of the energy-efficient equipment we use in our homes and businesses now, from lighting to heat pumps and laptops, runs on dc and the ac power coming into our buildings has to be converted to dc. With each conversion, energy is wasted.

As demonstrated in Fig. 1.2, the loss of energy conversion in buildings using ac power is significantly higher than in buildings using dc power. Therefore, integration of ac and dc power necessitates a transformative approach to energy routing, advocating for a unified infrastructure that can efficiently manage both ac and dc inputs.



(a) (b)

Figure 1.1 (a) Electricity generation trend from 2015 till 2050. (b) The trend of the energy consumption of buildings from 2015 till 2050 [2].

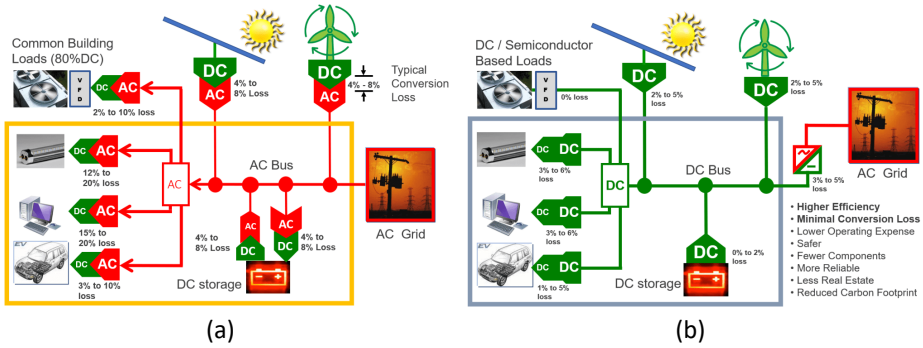


Figure 1.2. (a) Building based on ac input (b) The residential building based on dc input [3].

1.2 Motivation of the thesis

In the dynamic landscape of modern energy systems, the integration of diverse energy sources and the optimization of energy distribution have become critical imperatives. The coexistence of ac and dc technologies has emerged as a promising solution for achieving greater flexibility, efficiency, and resilience in energy systems. As a solution, the energy router for residential applications has terminals for both ac and dc source and loads.

Furthermore, the integration of advanced protection systems is essential to safeguard the energy router and the connected infrastructure against potential faults, surges, and other adverse events. The thesis will explore innovative protection mechanisms which provide a more reliable and safer performance of the device along with enhanced human safety.

By undertaking this research, the thesis aspires to contribute significantly to the advancement of energy infrastructure, facilitating the seamless integration of diverse energy sources while enhancing the reliability and protection mechanisms of the energy router. The outcomes of this work are expected to catalyze progress towards a more sustainable, efficient, and resilient energy future.

1.3 Aims, hypothesis and research tasks

The main aim of the PhD research is to develop and experimentally confirm a concept of a novel structure of energy router which is applicable for both types of the grids including dc and ac. It is being considered as solution which may speed up transition from conventional ac systems to the hybrid systems for using both ac and dc. The author sets the goal to utilize a smart power management system within the energy router structure along with increasing its safety and reliability.

Hypotheses:

1. Advanced solid-state circuit breakers provide completely safe operation of the energy router in case of a fault.
2. Common-ground interface solves the leakage current issue with no isolation requirements.
3. Fault-tolerant approaches increase reliability of energy router for residential application without significant redundancy.

4. Single-phase power electronic interface with smart internal relays and energy management algorithm is sufficient to balance three-phase single-family house supply system.

Research tasks:

1. Review of the fault-tolerant converters and lifetime management techniques.
2. Development of general structure and requirements for a new configuration of energy routers for residential applications with ac and dc terminals.
3. Evaluating common-ground interfaces suitable for industrial applications.
4. Design of advanced fault-tolerant ac/dc common-ground interface.
5. Design and analysis of reliable advanced solid-state circuit breakers for dc terminals with improved protection capability.
6. Experimental evaluation of the designed energy router prototype with low level control algorithms.

1.4 Research methods

The research methods used to carry out the thesis are based on mathematical analysis, simulation models and experimental verification. New developed topologies and circuits are mathematically analyzed using the MAPLE software. To study the operating properties of the new topologies and control algorithms, dynamic and static models are developed. Circuit simulations are performed in PSIM software. Altium Designer has been used for designing the circuit. All necessary software licenses have been provided by Tallinn University of Technology. Experimental investigation and validation of theoretically predicted results are performed using laboratory physical models of the new topologies including the energy router and two solid state circuit breakers. The Power Electronics Research Laboratory of TalTech has modern facilities (digital oscilloscopes and function generators, power quality and efficiency analyzers, microprocessor development tools, PCB prototyping, and assembling tools, etc.) for the hardware and software development.

1.5 Contributions and disseminations

The results of the research are approbated via scientific publications, conferences, symposiums, doctoral schools, and presentations. During the PhD studies the author contributed to 9 publications. Among them, 5 papers were published in peer-reviewed international journals including 4 papers as the first author. In addition, 4 papers were presented at international IEEE conferences. In total, the dissertation is based on 9 main scientific publications, including five journals and four conference papers presented at IEEE international conferences.

Scientific novelties:

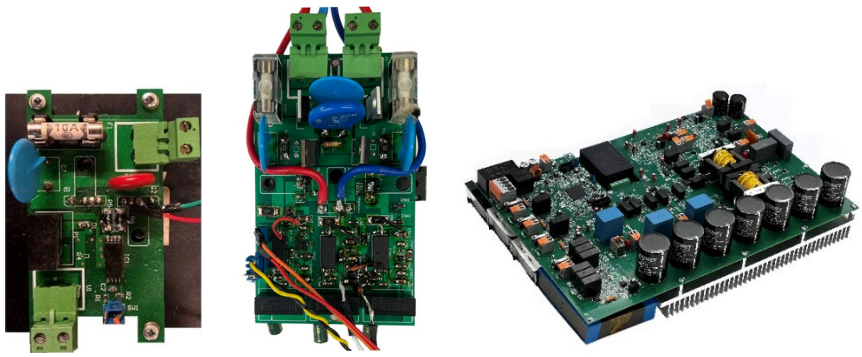
- Innovative classification framework based on a comprehensive review of lifetime management and fault management techniques.
- New configuration of three-phase energy router structure with single-phase power electronic interface.
- Novel solutions for solid-state circuit breakers improved protection capability.
- Novel fault-tolerant five-level common-ground inverter.

Practical contributions:

- Implementation of low-level control algorithms in experimental prototypes.
- Experimental verification of all solid-state circuit breakers.
- Experimental verification of the energy router.

1.6 Experimental setup and instruments

The experimental setups were assembled in power electronics laboratory of Taltech including the prototype of the SSCB with soft-reclosing capability as shown in Fig. 1.3(a), the SSCB with enhanced safety as shown in Fig. 1.3(b), and energy router the prototype of the energy router as shown in Fig. 1.3(c). The workspace in the lab and the prototypes are the lab are shown in Figure 1.4. The oscilloscope Tektronix MDO4034B-3 helps to catch the waveforms of voltages and currents of the passive components. The special probes Tektronix P5205A and Tektronix TCP0030A were used for voltage and current measurements correspondently. The Code Composer Studio is used as the environment for writing code for MCU from Texas Instruments, it was used during code development.



(a) (b) (c)

Figure 1.3 Power electronic circuits prototyped in power electronic laboratory of Taltech. (a) the SSCB with soft-reclosing capibility, (b) the SSCB with enhanced safety, (c) the energy router

1.7 Thesis outline

Chapter 2 describes the review of lifetime management techniques and fault-tolerant converters.

The principles of common-ground structures along with proposing two common-ground inverters including a fault-tolerant inverter are considered in Chapter 3.

In Chapter 4, an SSCB is proposed introducing a soft reclosing approach. In addition, a family of bidirectional SSCBs with increased safety is proposed, and the topologies are analyzed. The experimental results of these structures are included and discussed presenting the validity of the results.

Chapter 5 includes the description of the novel structure of the energy router. This chapter includes the experimental results of the various tests of the energy router.

2 Lifetime management techniques and fault-tolerant converters

Faults in power electronic systems may not only cause unscheduled interruptions, but they may also cause disastrous accidents that cannot be tolerated. Therefore, reliability is a fundamental aspect of power electronics design, ensuring safe, efficient, and consistent operation of electronic systems in various applications. Fig. 2.1. depicts the general guideline for the reliability of power electronic based systems. As shown in this diagram, a power converter's reliability can be discussed from two perspectives, including fault management and lifetime management. Both of these areas are typically considered separate subjects when it comes to research. Fault management is concerned with sudden catastrophic faults in converters, such as shorts and open circuits. It involves diagnosing, isolating, and configuring faults after they have already occurred in order to protect systems from faults. Another aspect of reliability is lifetime management, which involves analyzing, predicting, and extending the lifetime of power electronics.

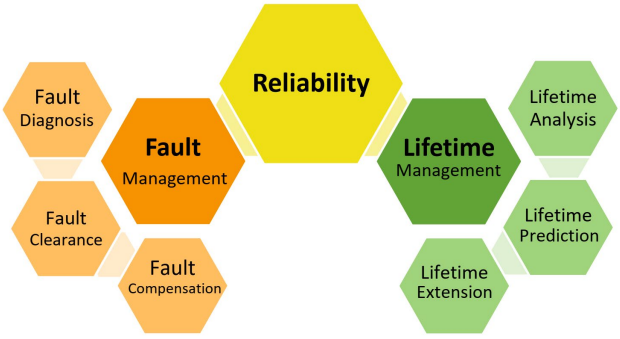


Figure 2.1 Guideline of the reliability of power electronic systems [4].

2.1 Lifetime management techniques

Lifetime management of power electronic systems is significant as it ensures optimal performance, reliability, and sustainability while reducing maintenance costs and extending system longevity. Lifetime management consists of three major categories: lifetime analysis, lifetime prediction and lifetime extension as shown in Fig. 2.2.

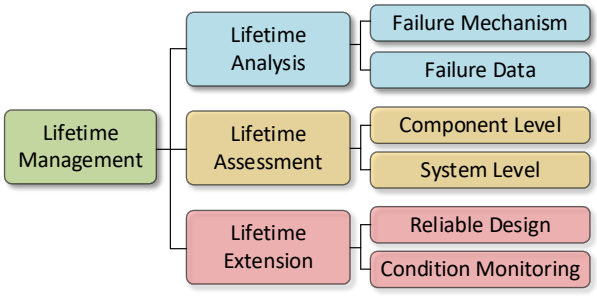


Figure 2.2 Guideline of lifetime management.

2.1.1 Lifetime analysis

Lifetime analysis is the fundamental step of lifetime management that involves identifying the prone-to-failure components along with the failure mechanisms, failure modes, failure causes, and failure indicators.

Among various power electronic based products, according to the pie chart shown in Fig. 2.3(a), the reliability of PV systems is severely affected by inverters. In fact, inverters are the most subject to failures with about 37 percent of the whole unscheduled maintenance. Because of their frequent on-off switching and the influence of thermal and electrical overstress, power semiconductors are more prone to failure than those in the rest of the drive system. As demonstrated in Fig. 2.3(b), these power devices such as IGBTs and MOSFETs account for about 31% of an inverter's failures and by considering the fault of the gate drivers, the total failure rate related to the switching devices is approximately 46%. Additionally, the figure shows that capacitors are the second most likely component to fail in power converters. If a converter lacks redundancy or reconfiguration, a failure of one of these components will cause the converter to fail, which is considered catastrophic in mission-critical applications.

Failures in Silicon Carbide (SiC) MOSFETs can be studied at the Chip-level structure (Fig. 2.4(a)) and the package-level structure (Fig. 2.4(b)). Chip-level failures in SiC MOSFETs are primarily due to gate oxide and body diode degradation, with gate oxide failure caused by tunnelling currents, high electric field stress, and high temperature stress, resulting in increased gate leakage current and threshold voltage shifts. Body diode failure is typically due to recombination-induced stacking faults from forward voltage bias stress, leading to higher forward voltage and drain leakage current. At the package level, failures often occur in bond wires and solder layers due to thermomechanical stress from CTE mismatch, humidity-induced corrosion, and high current density stress accelerating electromigration-related degradation [5]. Although various failure mechanisms have been identified, most current lifetime prediction models primarily address package-related failures.

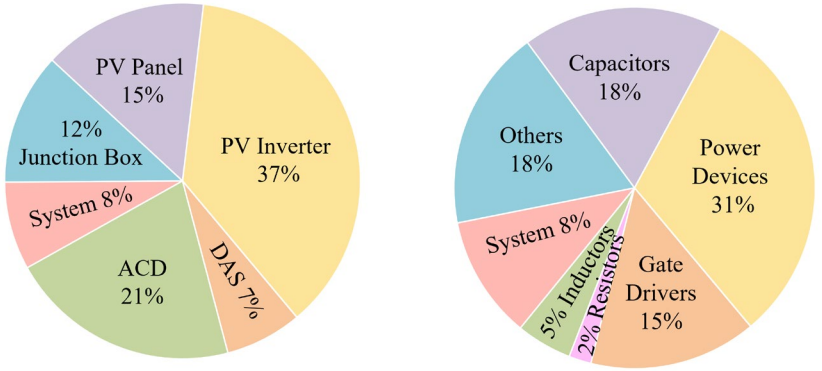


Figure 2.3 (a) Failure probability share of various parts of a PV plant. (b) Share of each component of a converter in converters' failure.

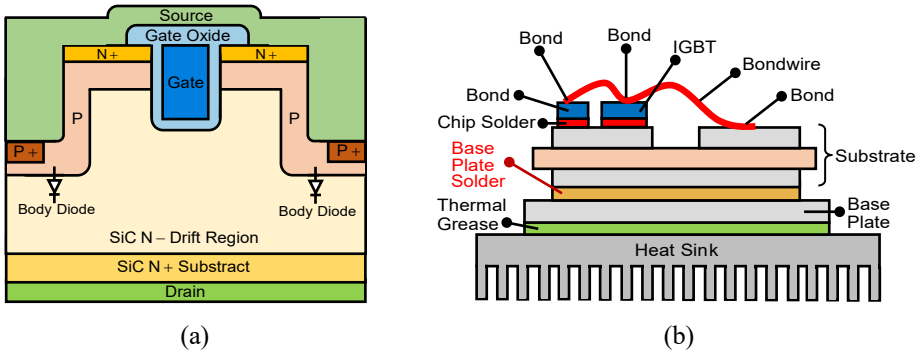


Figure 2.4 (a) SiC MOSFET chip-level structure. (b) SiC MOSFET package-level structure.

The failure data is the input for the lifetime prediction process. As demonstrated in Fig. 2.5, this failure data can be classified into three main categories: mission-profile based data, historical data, and data derived from accelerated tests, also known as test data. Mission-profile based data pertains to failure occurrences under actual operating conditions and specific use-cases, providing real-world insights into performance and reliability. Historical data encompasses records of past failures and maintenance logs, offering a comprehensive view of long-term trends and common failure patterns. Accelerated test data is obtained through rigorous testing procedures designed to simulate extended use or extreme conditions in a shorter timeframe, thereby identifying potential failure mechanisms and enhancing predictive accuracy. By integrating these diverse data sources, the lifetime prediction process becomes more robust and capable of providing reliable forecasts of system longevity and maintenance needs. The failure data is the input of the lifetime prediction process.

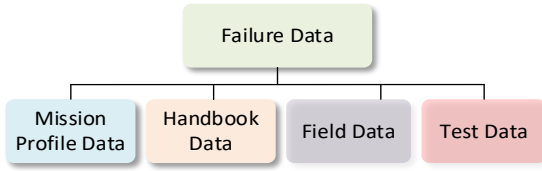


Figure 2.5 Different types of failure data for lifetime prediction process.

2.1.2 Lifetime assessment

The short lifetime of power electronic devices is usually caused by thermal stresses caused by their switching devices, such as IGBTs and MOSFETs. These components may fail due to a catastrophic failure (such as an open-circuit or short-circuit) or a wear-out failure, which affects the system's reliable operation. It is therefore necessary for converter manufacturers and operators to develop an appropriate assessment procedure to improve the reliability of converters, particularly the switching devices. [6].

The lifetime estimation of a power electronic system is first conducted using the component-level models to estimate the failure rate of each component. Afterwards, system-level lifetime estimates are generated based on the summed failure rates.

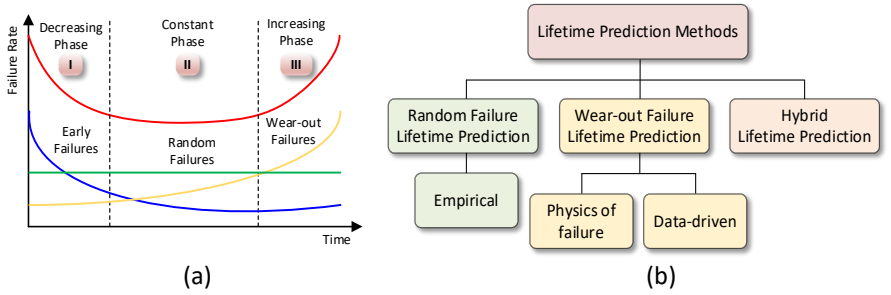


Figure 2.6. (a) Bathtub curve of the failure rate. (b) Classification of Lifetime Prediction Methods.

Reliability, unlike other conventional performance indicators for power electronic systems, like power density, efficiency, total harmonic distortion, etc., is hard to measure and quantify. The failure rate $\lambda(t)$ (also called hazard rate $h(t)$) is one of the widely used reliability metrics in reliability engineering. It is defined as the frequency with which a component or a system fails. Based on the conventional life cycle bathtub curve, as demonstrated in Fig. 2.6(a), there are three regions for the failure rate of electronics devices over time including early failures, constant random failures, and wear-out failures. The first part of the curve is dedicated to early failures. During this period, high numbers of failures occur as a result of errors in the design process or manufacturing procedures. The failure rate, however, decreases over time due to the removal of defective and failed products at the beginning of the stage. Early life failures can be addressed through burn-in or screening tests.

As depicted in Fig. 2.6(b), lifetime prediction methods can be classified into three categories: random failure lifetime prediction methods, wear-out failure lifetime prediction methods and hybrid methods which are applied by combination of the random and wear-out failure methods.

Empirical or handbook-based prediction methods are based on models developed from statistical curve fitting of historical failure data, which may have been collected in the field or from manufacturers. Typically, these methods provide reliability estimates for components with similar or slightly modified characteristics.

The most common handbook used for lifetime estimation is the Military Handbook 217. The general formula for calculating the failure rate (λ) in this method is as follows:

$$\lambda = \lambda_a . \pi_E . \pi_T . \pi_Q . \pi_J . \pi_S . \pi_R \qquad (2-1)$$

Where, λ_b is the base failure rate and other parameters are introduced in Fig. 2.7.

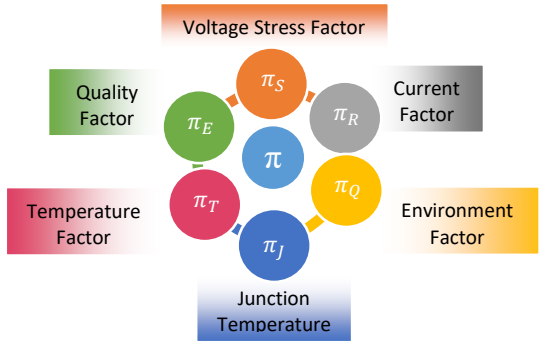


Figure 2.7. Failure parameters diagram.

Table 2.1 . Summary of major handbook standards.

	MIL-HDBK-217	IEC TR-62380	Telcordia	217plus	FIDES
Last Update	1995	2016	2006	2015	2009
Operation profile	NO	Yes	NO	Yes	Yes
Thermal cycling	NO	Yes	NO	Yes	Yes
Thermal rise in part	Yes	Yes	NO	Yes	Yes
Solder joints failures	NO	Yes	NO	Yes	Yes
Induced failures	NO	NO	NO	Yes	Yes
Failure rate data base for other parts	limited	limited	NO	Yes	Yes
Infant mortality	NO	Yes	NO	Yes	NO
Dormant failure rate	NO	NO	NO	Yes	Yes
Test data integration	Yes	Yes	NO	Yes	NO
Bayesian analysis	NO	NO	NO	Yes	NO

A summary of commonly used handbooks is provided in Table 2.1, and they are explained in detail in the same section that includes the table. Generally, MIL-HDBK-217 failure rate predictions are more pessimistic than other reliability handbook predictions. Some of these handbooks, like FIDES, are still used in some applications, despite the fact that their data is outdated, and their prediction approaches suffer from poor accuracy.

Compared to random failures' lifetime prediction methods, wear-out failures' prediction is often more complex and involves more steps. The diagram in Fig. 2.8(a) This figure illustrates a typical process for predicting wear-out failures. To do so, the first step is to collect failure data from various sources, including mission profiles, testing data, and field data. The next step, if using mission-profile data, would be to translate this data into a thermal profile using electrothermal modelling. Upon completion of the cycle counting process, a suitable lifetime model should be selected in order to calculate the number of failures per cycle. To obtain a precise result, the deviation of the output parameters after the damage accumulation is estimated. Finally, reliability is demonstrated by either Cumulative Distribution Function (CDF) or Probability Density Function (PDF).

The fundamental step in the mission profile-based reliability prediction is translating the converter's mission profile to the corresponding stresses in its prone-to-failure components [7]. Fig. 2.8(b) shows the three steps to translate the mission profile to achieve the junction temperature change.

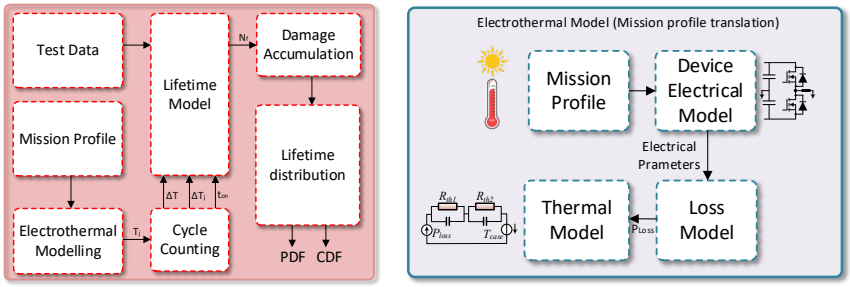


Figure 2.8. (a) General diagram of a typical component-level lifetime prediction process. (b) General diagram of a typical electrothermal model.

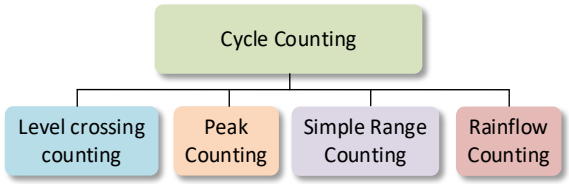


Figure 2.9 Methods of cycle counting.

The next step is cycle counting. A power converter's lifetime is determined by the magnitude and frequency of temperature cycles. Each cycle applies different stresses to the module and results in a particular consumed lifetime. Cycle counting summarizes lengthy irregular load-versus-time histories by providing the number of times cycles of various sizes [8]. The definition of a cycle varies with the method of cycle counting. Several cycle counting methods have been developed for lifetime prediction, three of which are level crossing counting, peak counting, range counting, and rainflow counting.

After cycle counting, it is time to model the lifetime. Fig. 2.10 classifies the wear-out failure lifetime prediction methods and demonstrates the major techniques used in each method. PoF offers better accuracy since the failure rates are calculated based on the actual physics of the components and their failure modes and mechanisms along with the effect of stresses of the product-level on the reliability of the components. There are also data-driven methods in which models are typically "black boxes" with no explicit system knowledge. Data-driven approaches involve learning statistical relationships and patterns from the failure data to provide valuable decision-making information.

Damage accumulation is the next step. Once the damage caused by each thermal cycle has been determined, the total accumulation of damage is calculated, and an estimation of its lifetime can then be obtained using either linear or nonlinear methods. [9]. One of the commonly used methods in damage accumulation evaluation is Palmgren-Miner law [10, 11].

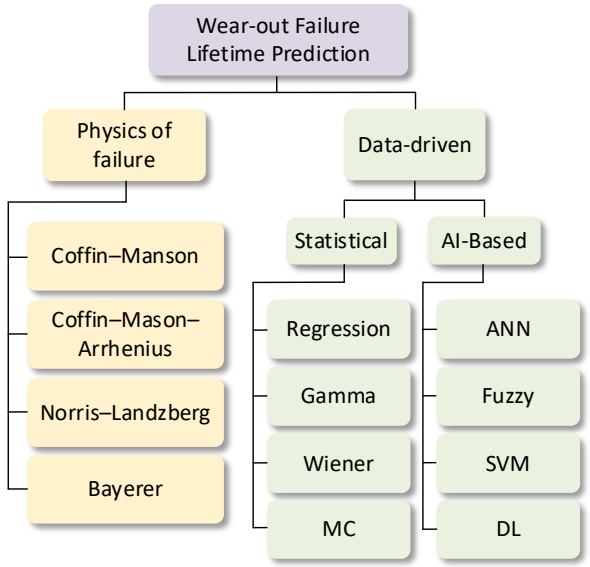


Figure 2.10 Methods of predicting the wear-out failure lifetime.

The formula for calculating the damage accumulation by this method is as follows:

$$AD = \sum_{k=0}^{n} \frac{n_i}{N_i}, \qquad (2-2)$$

where N stands for the total number of power cycles generated by the rainflow counting algorithm, n_i is the number of cycles for i^{th} power cycle, N_i is the number of cycles to failure at the corresponding ΔT_j and T_m in the i^{th} power cycle [12].

The last step of lifetime prediction is parameter estimation and lifetime distribution. The basic idea of parameter estimation is modelling the parameters used in the calculation (e.g., stress parameters in a lifetime model) using a certain distribution function (f(x)), instead fixed parameters [8] with a range of variations (e.g., normal distribution with 5% parameter variation). Thus, uncertainty in practical applications can be represented by parameter variations in the calculation. Monte Carlo simulations are widely used for analyzing the stochastic behavior of model parameters, which represents uncertainty in the prediction [13]. They are based on simulating the model parameters with a certain distribution, representing variation, and randomly selecting them during each simulation.

Afterwards, a set of n samples is carried out to evaluate the lifetime. In this way, the lifetime distribution (e.g., Weibull distribution) of a power electronic component can be constructed based on the lifetime yields of n samples [14].

When the lifetime prediction of all components of a system is determined, one of the system-level lifetime prediction methods is used to map the reliability of the components to the systems. These system-level methods include Reliability Block Diagrams (RBD), Fault-Tree Analysis (FTA), and Markov Chains (MC) [15].

2.1.3 Lifetime extension

Design for Reliability (DfR) and condition monitoring are integral tools in extending the lifetime and enhancing the reliability of power electronic systems, which are critical in applications ranging from renewable energy to industrial automation.

DfR involves incorporating reliability considerations into the design phase, aiming to predict, quantify, and mitigate potential failure modes early in development. This approach includes careful component selection to ensure that only high-quality, durable components are used, capable of withstanding the environmental and operational stresses they will encounter. Effective thermal management strategies, such as employing heat sinks, cooling fans, and advanced materials, are crucial for dissipating heat and maintaining optimal operating temperatures, thereby preventing thermal degradation of components.

Furthermore, DfR emphasizes robust design principles and redundancy. By incorporating redundancy, systems can maintain functionality even if one component fails, enhancing overall resilience. Derating, or operating components below their maximum capacity, along with planning for worst-case scenarios, further bolsters system reliability. Implementing Failure Mode and Effects Analysis (FMEA) systematically identifies potential failure modes, their causes, and their effects on system performance. Addressing these potential issues during the design phase enables engineers to incorporate necessary countermeasures. Accelerated Life Testing (ALT) exposes components to elevated stress conditions, providing valuable data on potential failure mechanisms and lifespan, which informs design improvements and reliability predictions.

Condition monitoring provides continuous assessment of the system's health and performance during its operational life. This involves using sensors to measure critical parameters such as temperature, voltage, current, and vibration, supplying real-time data essential for monitoring the system's condition. Advanced data analysis and diagnostic algorithms, including machine learning techniques, analyze this data to detect anomalies and diagnose issues early. Predictive analytics can forecast potential failures, allowing for proactive maintenance and timely interventions. Health monitoring systems integrate sensor data and diagnostic tools, offering a comprehensive overview of system health and alerting operators to degrading conditions, thus recommending maintenance actions to prevent failures.

Prognostics further enhances condition monitoring by combining real-time data with models of system behavior to predict the Remaining Useful Life (RUL) of components. This predictive capability facilitates better planning of maintenance schedules, minimizing downtime and extending the system's operational life. The synergy between

DfR and condition monitoring creates a robust framework for managing the lifecycle of power electronic systems. By integrating these methodologies, organizations can significantly reduce unexpected failures, optimize system performance, and lower costs associated with maintenance and downtime. Prioritizing reliability through both design and continuous monitoring leads to more robust and durable power electronic systems, capable of delivering consistent performance over extended lifetimes.

2.2 Fault tolerant converters

Fault tolerant converters are a crucial advancement in the field of power electronics, designed to enhance the resilience and reliability of electrical systems by ensuring continuous operation even in the presence of faults. As the demand for uninterrupted power supply grows in critical applications such as renewable energy systems, electric vehicles, and aerospace technologies, the ability of converters to handle and adapt to failures becomes increasingly vital. These converters incorporate sophisticated design strategies, including redundancy, robust control algorithms, and self-healing mechanisms, to detect, isolate, and mitigate faults without significant interruption. When a fault occurs, the fault management operation is activated which consists of fault diagnosis, fault isolation and fault compensation.

Once a fault occurs, fault diagnosis or fault detection is the first step. A fault diagnostic technique for an inverter can be categorized as model-based or data-driven [16]. The model-based methods are based on the analytical model of the converter [17]. Usually, they need to consider the dynamic properties and operation mechanism of the system before establishing an accurate mathematical model [18]. On the other hand, it is not necessary to know the analytical model of the system to use data-driven fault diagnosis methods as they directly analyze and process the measured data [19]. These techniques include signal processing methods, statistical analysis, and artificial intelligence. In addition to these two methods, the hybrid method uses a combination of these two methods.

Fault isolation is the second step in tackling a fault in a system. When a fault occurs in an inverter, some switching states may be unavailable due to the short-circuit or open circuit of the faulty switches. These switching states should be avoided or the faulty components themselves should be isolated so that the system continues to function and prevents damage to the entire system. These schemes are performed by adding some extra elements such as fuses and TRIACs and their goal is to isolate the faulty switch(es).

Fault isolation usually results in the degradation of the system's performance, especially in the output voltage and Total Harmonic Distortion (THD). Therefore, there have to be solutions to compensate for the effects of the fault which are discussed in section III.

Having isolated the fault, fault compensation schemes are needed to restore the inverter's operation as closely as possible to normal. As shown in Fig. 2.11, fault compensation techniques are classified into three groups: hardware redundancy, switching states redundancy, and unbalance compensation control. An output performance measure such as THD of output voltages and currents, efficiency of the system, and dynamic response should be considered when selecting a fault-tolerant method. Aspects such as cost are also important to consider when comparing fault compensation techniques.

2.2.1 Hardware redundancy

A redundancy scheme is one in which a system feature that is unavailable can simply be replaced with another feature already present [20]. There are two kinds of redundancy in inverters: switching state redundancy, which involves alternative current paths to obtain the same voltage level, or hardware redundancy, which involves extra switches, legs, and modules. The redundant hardware technique involves adding some redundant hardware to the original system. In applications where cost is not a major concern, redundant hardware can be added to the system to provide advantages in post-fault operations [21].

In the switch-redundant topology in Fig. 2.12(a), if one of the upper switches fails open-circuit or short-circuit, it can be replaced by the redundant switch S_{R1} by the correspondent relay. The strategy for the failure of the bottom switches is the same.

As shown in Fig. 2.12(b), some hardware redundant topologies use the redundancy of a whole leg to make the leg replicable when a probable fault occurs. The redundant leg can be connected in parallel or in series.

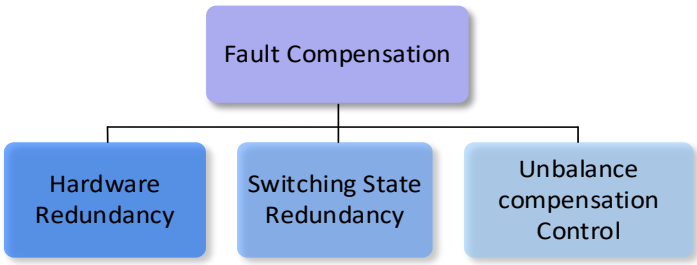


Figure 2.11 Classification of fault Compensation techniques for power converters.

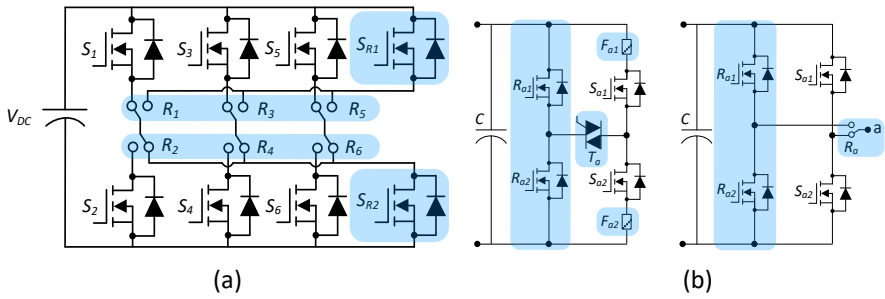


Figure 2.12 (a) Fault-tolerant inverter using parallel switch redundancy proposed in [22]. (b) Fault tolerant topologies using leg redundancy.

2.2.2 Switching states redundancy

Modulation-based fault clearance includes avoiding the unavailable switching states and minimizing the impact of the fault by a proper switching sequence [23]. In this approach, in case of failure, redundancy in the switching states of the inverter enables the controller to choose an alternate conduction path to retain the same output voltage.

In the three-phase NPC inverter of which the leg "a" and its corresponding phase is shown in Fig. 2.13(a), when one of the switches fail, the faulted state should be avoided because it causes a short-circuit across the bottom or top dc-bus. In the SVM technique, it is enough to exclude the vectors including the faulted phase. With this approach, the fault is cleared, however, the modification of the PWM strategy to avoid unavailable states leads to dc-bus mid-point imbalance, spurious fault detection, and overrating of device voltage to full dc-bus voltage [24].

Active Neutral Point Clamped (ANPC) converter, which is obtained by replacing diodes in NPC with switches, is widely used in high-power medium-voltage applications including distributed generation such as photovoltaic systems, motor control in traction systems, and industrial motor drives [25]. In this converter as shown in Fig. 2.13(b) [26, 27], if an open-circuit fault occurs in the switch S_{a2}, the switches S_{a3} and S_{a6} can be turned on to connect the phase voltage to the dc-bus mid-point which minimizes the impact of the fault by reviving the three-phase system.

In the flying capacitor inverter as shown in Fig. 2.13(c), in the normal mode, the voltage level can be provided by turning on switches S_1, S_3, and S_4 (the current flows through the capacitor C_2 and diode D_2). If for example the switch S_3 fails open, while i_L>0, the same voltage level can be obtained by turning on the switches S_4 and S_1 (the current flows through the capacitor C_3 and diodes D_2 and D_3). On the other hand, in the healthy condition, turning on the switch S_2 (the current flows through capacitors C_1 and C_2, and the diodes D_1, D_3, and D_4) the voltage level is produced. If S_3 fails short, while i_L<0, the same output voltage is obtained when current flows through diodes D_1 to D_4. Therefore, the flying capacitor inverter benefits from the switching state redundancy which makes it retain its output voltage level after an open-circuit or short-circuit fault occurs.

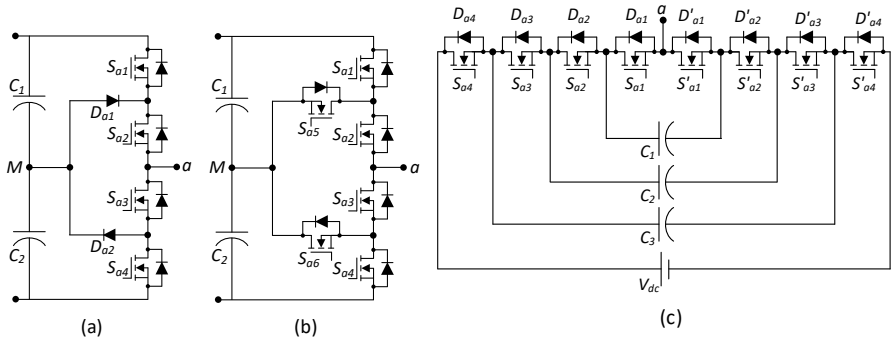


Figure 2.13 (a) One leg of a three-phase NPC inverter, (b) One leg of a three-phase ANPC inverter, (c) Flying capacitor inverter.

2.2.3 Unbalance compensation control

Despite the fact that the most important function of an inverter when a fault occurs is to continue servicing as close to normal as possible, other features should also be considered [28]. Imbalance control techniques refer to the altercation of the control strategy to correct the imbalances created by the fault and achieve an optimum operating point concerning the voltage, THD, or any other objective [29]. By using this algorithm, fault-tolerant control can be implemented without changing the inverter's topology. As a result, using them can save hardware costs and simplify topologies [30].

In Neutral Phase Shift (NPS) method, when a fault occurs in a module in a Modular Multilevel Converter (MMC) or Cascaded Multilevel Converter (CMC), one option after isolation of the faulty module is isolating the corresponding modules in the other two phases to keep the output voltage balanced. However, the output voltage is reduced.

By using the NPS method, there is no need to bypass the corresponding healthy modules and have a balanced output at the same time. As shown in Fig. 2.14(a), the line-to-line voltages in normal operation are 8.67 p.u.

When modules W_4, W_5, and V_5 experience a fault, the correspondent healthy modules, which are V_4, U_4, and U_5 are bypassed. The new line-to-line voltages are 5.19 p.u. (Fig. 2.14(b)). By solving the following equations, we can find the angles between phases that make the voltage balanced [31].

$$V_{ab} = {V_a}^2 + {V_b}^2 - 2V_aV_b\cos(\alpha)\,, \qquad (2-3)$$

$$V_{bc} = {V_b}^2 + {V_c}^2 - 2V_bV_c\cos(\beta)\,, \qquad (2-4)$$

$$V_{ca} = {V_c}^2 + {V_a}^2 - 2V_cV_a\cos(\gamma)\,, \qquad (2-5)$$

$$V_{ab} = V_{bc} = V_{ca}, \qquad (2-6)$$

$$\alpha + \beta + \gamma = 360^{\circ}. \qquad (2-7)$$

As shown in Fig. 2.14(b), the output voltage is higher than the conventional method.

This method is similar to the NPS technique with the difference that the output voltage can be sustained at the same level as that in the pre-fault condition [32, 33]. An important drawback of the previous reconfiguration strategy is its effect on the common-mode voltage, which can lead to unbearable stress on the machine bearings [34].

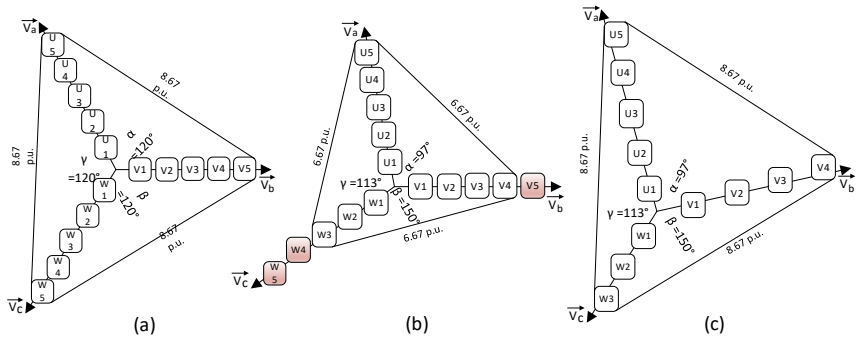


Figure 2.14 The voltage vectors of a modular multilevel inverter (a) Normal Condition, (b) Postfault after implementing NPS approach. (c) Postfault; the overvoltage is shared among three phases.

Voltage extension is another control method for fault management in modular converters. To increase the converter's maximum output range, the average of the maximum and minimum reference phase voltages is injected into the common-mode voltages. When a fault occurs, in order to maintain the output voltage level, the input dc-bus voltage of the faulty phase is increased to keep the total voltage unchanged. As shown in Fig. 2.14(c), the three voltages are balanced, and their value is the same as the normal operation. However, the modules in the phase which had the faulty modules, experience overvoltage. Therefore, to equally share the increased voltage burden among all healthy modules of three phases and optimal angles of the phase voltages are calculated by equations (2-3) to (2-7).

2.3 Summary

The reliability of power electronic systems is crucial to ensure safe and uninterrupted operation in various applications, necessitating comprehensive fault management and lifetime management strategies. Fault management focuses on diagnosing, isolating, and compensating for sudden catastrophic faults, while lifetime management involves analyzing, predicting, and extending the operational life of the systems. Techniques such as DfR and condition monitoring play key roles in enhancing system durability by integrating robust design principles and real-time health assessments. Fault-tolerant converters, which incorporate redundancy and advanced control algorithms, are essential for maintaining continuous operation amidst failures. These converters leverage methods like hardware redundancy, switching state redundancy, and unbalance compensation control to mitigate faults effectively. Voltage extension methods further aid in managing faults by adjusting phase voltages to maintain output levels, thereby ensuring consistent and reliable performance of power electronic systems.

Findings of this section denies the third hypothesis that fault-tolerant approaches increase reliability of energy router for residential application without significant redundancy, since control techniques without redundancy only compensate imbalance in the performance of the converters and cannot fully compensate and clear the fault.

3 Common-ground structure

Despite dc microgrids' advantages, such as flexibility in integrating renewable sources and higher efficiency, they require high protection. Even though dc microgrids have advantages, including higher efficiency, they will be impractical without a reliable protection system. DC system protection is different from that of an ac system. A dc system is protected differently from an ac system. DC systems have many active sources, and each of these sources has a different power level that should be taken into account in comprehensive protection systems. The dc current fault in the dc microgrid increases suddenly during a fault, and since it does not have a zero crossing, it cannot be easily cut; it requires additional equipment to do so [35]. Consequently, there are several aspects to consider from a protection perspective. Only a few studies have been conducted on dc system protection in recent years. [36]. The dc system continues to develop at a slow pace due to a lack of necessary standards and sufficient experience. A dc microgrid can operate independently or in a grid-connected mode, as well as bi-directionally. These operation modes also introduce more challenges to the protection system. It is also important to consider issues related to grounding and the ground current when diagnosing high impedance faults [37].

Capacitive grounding methods (Fig. 3.1(a)) offer advantages such as providing a low-impedance path for common-mode currents to ground, effectively reducing leakage current and enhancing system safety. They are relatively simple to implement and can be cost-effective compared to other grounding techniques. Capacitive grounding methods also do not introduce additional components or losses into the power circuit, which can help maintain system efficiency. However, they may be less effective in high-frequency applications where capacitive coupling with ground can result in increased EMI. Additionally, proper sizing and placement of capacitors are essential to prevent excessive leakage currents and ensure compliance with safety standards. Moreover, capacitive grounding methods may not be suitable for all applications, particularly those with stringent EMC requirements or where galvanic isolation is necessary.

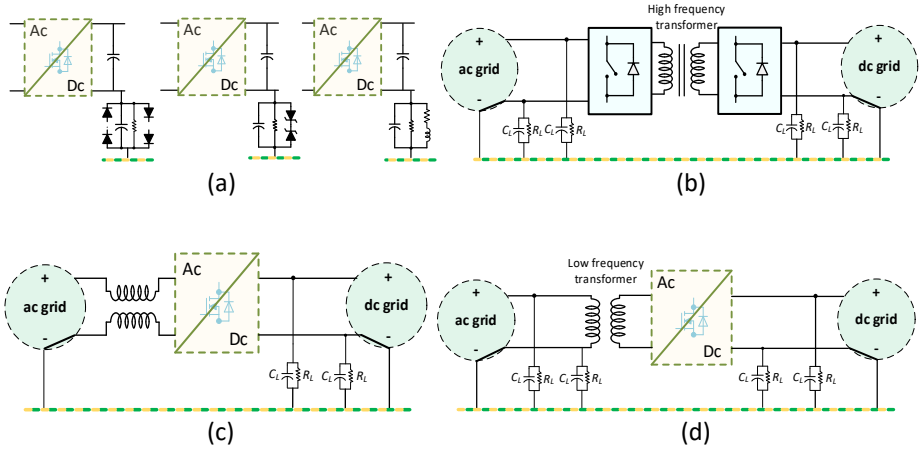


Figure 3.1 Typical solutions to address the leakage current: (a) capacitive grounding methods, (b) high-frequency transformer at the dc side, (c) common-mode choke, (d) a low-frequency transformer at the ac side.

Using a high-frequency transformer at the dc side (Fig. 3.1(b)) to address leakage current in power electronic systems presents advantages such as efficient isolation, which can effectively suppress leakage currents and enhance system safety. High-frequency transformers also offer compact size and reduced weight compared to their low-frequency counterparts, making them suitable for applications with space constraints. Moreover, they allow for higher power density and improved efficiency due to reduced core losses. However, high-frequency transformers may introduce higher Electromagnetic Interference (EMI) and require careful design considerations to minimize losses and maintain high efficiency [38]. Additionally, they may be more expensive and necessitate precise control and protection mechanisms to ensure reliable operation.

Using a common-mode choke at the ac side (Fig. 3.1(c)) to address leakage current in power electronic systems offers advantages such as effective reduction of common-mode noise, which can enhance system reliability and compliance with regulatory standards. Additionally, common-mode chokes can provide protection against ground loops and are relatively simple to implement. However, they come with drawbacks including added cost, size, and weight, as well as potential voltage drop and limited frequency range.

Using a low-frequency transformer at the ac side (Fig. 3.1(d)) to address leakage current in power electronic systems offers advantages such as robust isolation, which effectively suppresses leakage currents and enhances system safety. Low-frequency transformers are known for their reliability and ability to handle high power levels, making them suitable for various industrial applications. Additionally, they typically have lower core losses and produce less EMI compared to high-frequency transformers. However, low-frequency transformers tend to be larger and heavier than their high-frequency counterparts, which may pose challenges in applications with strict space and weight constraints. Moreover, they may exhibit lower efficiency due to higher core losses, necessitating careful design considerations to optimize performance and minimize energy losses.

As demonstrated in Fig. 3.2, a common-ground structure in power electronic systems helps suppress leakage currents primarily by providing a low-impedance path for unwanted currents to return to the power source or ground. By establishing a single reference point for grounding, the common-ground structure ensures that all components share the same ground potential. This reduces the likelihood of voltage differentials between components, which can lead to leakage currents flowing through unintended paths. Additionally, a well-designed common-ground structure minimizes ground loops and reduces electromagnetic interference, further contributing to the suppression of leakage currents. Overall, by promoting a stable and uniform grounding environment, a common-ground structure helps maintain system integrity and safety while mitigating the risks associated with leakage currents.

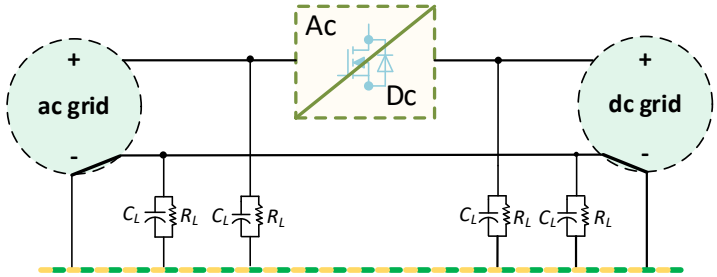


Figure 3.2 Common-ground technique to suppress the leakage current.

3.1 The three-level common-ground inverter

Fig. 3.3 shows the three-level common-ground inverter implemented in the structure of energy router, which consists of five switches, an inductor in series to the input voltage, and a flying capacitor. The converter is common ground as the neutral point of the output side is directly connected to the negative polarity of the input side. The operating states of the inverter are demonstrated in Fig. 3.4. In the first operating state in Fig. 3.4(a) in which the level $+V_O$ is produced, the inductor is in the charging state, while the capacitor is discharged. The operating states in which zero levels are provided are shown in Figs. 3.4(b) and 3.4(c). Once S_1 is turned ON; the current of the inductor ramps up. Once S_2 is triggered to turn ON, the stored energy in the inductor goes down to charge the capacitor. The level $-V_O$ is produced in the operating state in Fig. 3.4(d) in which the capacitor is charging and the inductor discharging. One advantage of this structure is the fixed duty cycle during the boost operation, which simplifies the control strategy. A detailed modulation strategy can be found in [39].

In this converter, the step-up mode works according to the boost converter with a duty cycle of D. Therefore, the ratio of capacitor voltage to the dc input voltage is equal to:

$$V_C = \frac{1}{1-\mathrm{D}} V_{dc}, \qquad (3-1)$$

Where D is the duty cycle of the boost part and corresponds to S_2, which is responsible for the boosting part of the converter. The output ac voltage is also as:

$$V_O = \mathrm{M} V_C \sin(\omega t)\,, \qquad (3-2)$$

where M is the modulation index and corresponds to the amplitude of the sine wave with the same frequency as the output voltage. Also, the peak of fundamental ac output is:

$$V_{O,max} = \mathrm{M} V_C. \qquad (3-3)$$

Finally, the ac to dc gain is expressed as:

$$\mathrm{G} = \frac{V_{O,max}}{V_{dc}} = \frac{\mathrm{M}}{1-\mathrm{D}}. \qquad (3-4)$$

In the modulation of this converter, D is always greater than M. After calculating M and D for the desired output, these values should be the output of the control system to produce PWM Pulses. Having D and M, the four operating states are produced through the modulator.

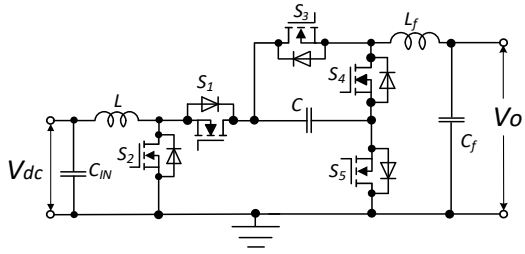


Figure 3.3. Three-level common-ground flying capacitor-based solution to address the leakage current.

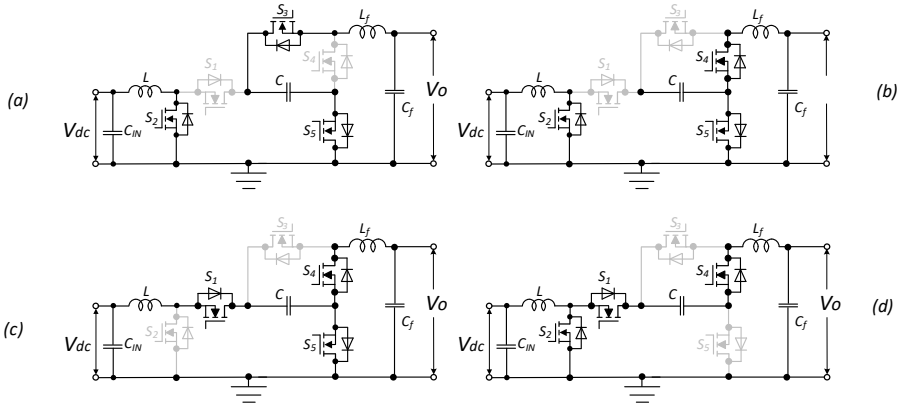


Figure 3.4 Equivalent circuits of the three-level common-ground flying capacitor-based solution. (a) $V_O = +V_C$, (b) $V_O = 0$, (c) $V_O = 0$, (d) $V_O = -V_C$.

The controller of the inverter as shown in Fig. 3.5, includes a Phase-Lock-Loop (PLL) and a Proportional Integral (PI) controller along with a Proportional Resonance (PR) controller are used to produce modulation index (M) and duty cycle (D) required by the inverter. PLL samples grid voltage and provides synchronization to the primary grid. For this PLL, the traditional Second Order Generalized Integrator (SOGI) regulator is used. The grid side reference current (I^*_g) is derived by means of a PI controller using the reference value (V^*_{dc}) and the actual value (V_{dc}) of the dc input voltage. Finally, a conventional PR controller is used for grid current control, producing M and D using the reference ($I^*_g(t)$) and the actual grid current ($I_g(t)$).

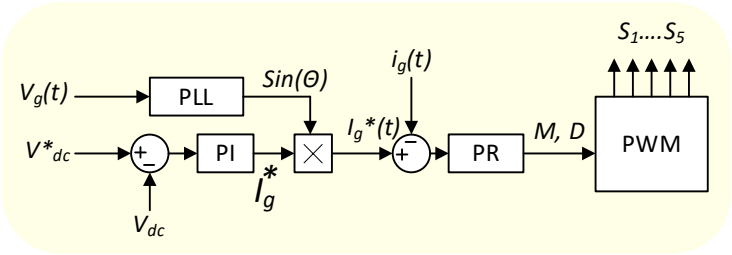


Figure 3.5 The block diagram of the applied control system.

3.2 The proposed five-level fault-tolerant inverter

The proposed fault-tolerant inverter is demonstrated in Fig. 3.6. It comprises of a total of ten power semiconductor switches, an inductor, and two flying capacitors (C_1 & C_2). The proposed topology produces nine-level output voltage waveform across the load terminal with $\pm V_{dc}$, $\pm 2V_{dc}$, and zero voltage levels under healthy conditions.

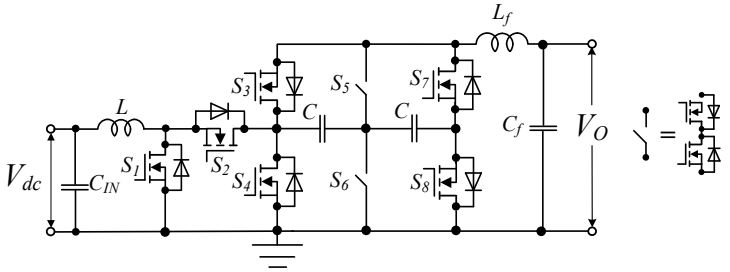


Figure 3.6 The proposed five-level common-ground fault-tolerant inverter.

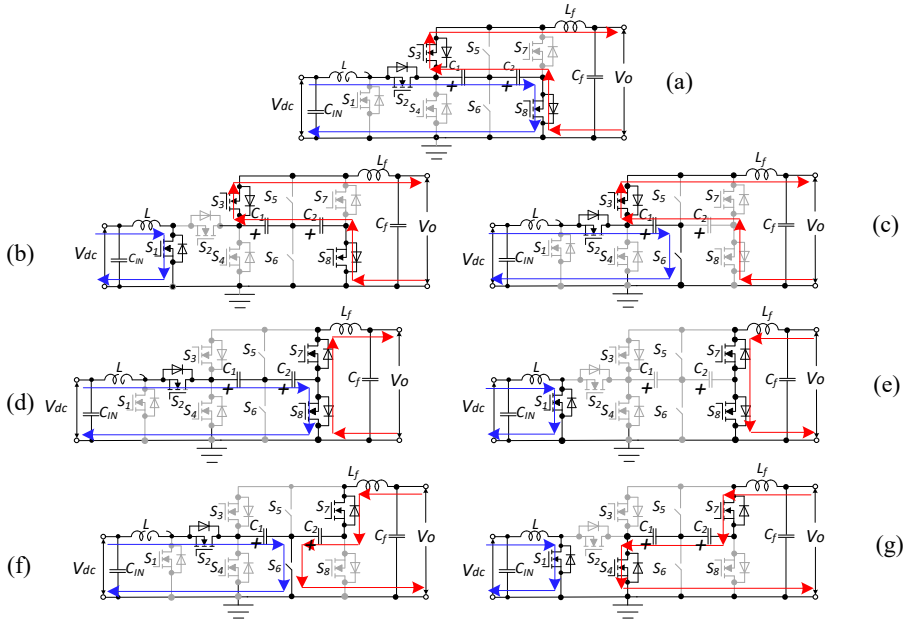


Figure 3.7 Operating states of the proposed fault-tolerant inverter. (a) $V_O = +2V_C$, C_1 & C_2: charging, L: discharging, (b) $V_O = +2V_C$, C_1 & C_2: discharging, L: charging, (c) $V_O = +V_C$, C_1: charging, L: discharging, (d) $V_O = 0$, C_1 & C_2: charging, L: discharging, (e) $V_O = 0$, L: charging, (f) $V_O = -V_C$, C_1: charging, L & C_2: discharging, (g) $V_O = -2V_C$, C_1 & C_2: discharging, L: charging.

There are seven operating states as demonstrated in Fig 3.7. In mode (a) as shown in Fig. 3.7 (a), capacitors C_1 & C_2 are charging while in mode (b) in Fig. 3.7 (b) these capacitors are discharging and, in both modes, the voltage $+2V_C$ is provided in the output. In mode (c), inductor L is transferring its power to the capacitor C through switches S_2 and S_6 to provide the voltage $+V_C$ in output terminals. In modes (d) and (e), zero output voltage is provided by turning on S_7 and S_8 simultaneously. In mode (f), while C_1 is

charging, C_2 is discharging in the load and makes the output voltage of -V_C. In the last mode in Fig. 3.7 (g), Both capacitors are discharging, and the inductor L is charging and -2V_C is provided in the output.

The fault-tolerant operation of the inverter works such that if any of the three legs of this inverter experiences a fault, or if any of the switches fails, the inverter can be converted into the three-level inverter in Fig. 3.3. Any of the short-circuit faults can be converted to open circuit using fault isolation techniques.

3.3 Comparative analysis

In this section, the aim is to compare the presented inverter in Fig. 3.3 with similar ones in recent literature. These solutions include the unfolding circuit with a buck–boost converter from [40], and the flying inductor power converter in [41], along with the five-level switched capacitor inverter proposed in [42] and the FI-based power converter from [43]. The schematics of these solutions are shown in Figure 3.8. All of these solutions are common ground, except for the buck–boost converter and the unfolding circuit from [40]. While the unfolding circuit can significantly reduce leakage current, it cannot eliminate it entirely.

In the presented inverter, a dual-purpose power converter is introduced. Based on the flying capacitor circuit, it operates as a three-level inverter. A capacitor is used to pump energy into the negative output voltage. On the other hand, the inverter in [42] is based on the switched capacitor circuit and uses two capacitors as voltage sources in the negative half cycle. Despite the fact that virtual voltage sources are used in power converters, their methods of charging capacitors differ. In the presented inverter, the capacitor charges smoothly via a charging inductor, while in [42], the capacitors charge directly from the voltage source at the switching frequency, resulting in spikes in current. In contrast, the unfolding circuit in [40] uses a virtual capacitor that functions as a current source.

Similar to the selected dual-purpose flying inductor converter, the introduced power converters in [41, 43] are based on flying inductor circuits, and the required energy is pumped from the inductors to the output. Among the compared topologies, the switched capacitor power converter in the presented inverter has a fixed double-voltage boosting capability, while other solutions can operate under a wide range of input voltages.

In order to discuss the advantages and disadvantages of each structure, it should be noted that each structure is designed and tested under different conditions; hence, it is not possible to make a fair comparison. However, the fundamental waveforms of a typical converter are independent of the component type and electric parameters (e.g., switching frequency and selected semiconductors). To put it differently, the primary wave forms are produced through the fundamental modulation method, which establishes certain overall requirements for component sizing. These requirements involve estimating passive component values, which can be achieved by considering equal current ripples in the inductors and identical voltage ripples across the capacitors.

In Eqs. (3-5) and (3-6) the maximum accumulated energy inside a capacitor and an inductor are calculated, respectively. According to these equations, the volume of a core of an inductor as well as the volume of a capacitor can be estimated:

The volume of a core of the inductor as well as the volume of the capacitor can be estimated based on its maximum accumulated energy.

$$Vol_C = W_C = \sum_{i=1}^{N_C} C_i {v_{Ci}}^2 , \quad (3-5)$$

$$Vol_L = W_L = \sum_{i=1}^{N_L} L_i {i_{Li}}^2 , \quad (3-6)$$

where, L_i and C_i are values of i^{th} inductance and capacitor, N_L is the number of inductors and N_C is the number of capacitors. i_{Li} is the peak inductor current and v_{Ci} is the peak capacitor voltage.

Also, we introduce the relative conduction losses that are independent of the selection of semiconductors. The relative conduction losses are proportional to the square of the switch current. As a result, total conduction losses can be scaled to:

$$P_{CON} = \sum_{i=1}^{N_S} {i_{Si}}^2 . \quad (3-7)$$

Finally, we can estimate the Total Standing Voltage (TSV) across the semiconductors:

$$TSV = \sum_{i=1}^{N_S} V_{Si} . \quad (3-8)$$

Based on the above-mentioned points, the same condition is provided for all the selected topologies in PSIM environment under equal condition as the following.

The inductors were selected to have the current ripple equal to 20% of their current ratings. With this assumption, the used charging inductor in [40], are 3.3 mH, the two inductors in the flying inductor power converter in [41] are 1 mH, the inductor in the flying inductor power converter in [43] is 1.1 mH, and the inductor in the selected converter is 1mH.

The capacitors were selected to have the voltage ripple equal to 10% of their voltage ratings. With this assumption, the used capacitor is 10 µF in the flying capacitor based power converter in the presented inverter, is 2 µF in the buck-boost and the unfolding circuit in [40], is 300 µF in the flying inductor based power converter in [41], is 1600 µF for C_1 and 680 uF for C_2 in the switched capacitor based inverter in [42].

The output filter for the selected converter, the flying inductor based converter in [41], the flying inductor based converter in [43], and the buck-boost and the unfolding circuit in [40] is a CL type. The output filter for the flying capacitor based power converter in presented inverter and the switched-capacitor inverter in [42] is a CL type. In all the compared topologies, the output filter capacitor is 3.3 µH. It should be noted that the used capacitor in the unfolding circuit acts as the output filter capacitor and is equal to 2 µF. There is no additional output filter capacitor in this topology. In the selected topology, the inductance of the output filter inductor is 500 µH. It results in 2.53 % THD in the output current. Hence, the output filter inductors are selected to have the same THD. in the output current. Based on this assumption, the output filter inductor is 750 µH for the buck-boost and the unfolding circuit in [40], is 1700 µH for the flying capacitor based power converter in the presented inverter, is 1 µH for the flying inductor based converter in [41], is 700 µH for the flying inductor based converter in [43], is 2000 µH for the switched capacitor based power converter in [42].

The following parameters were considered for all the compared topologies to simulate the same condition: Input voltage (V_{IN}) = 200 V, peak value of the output voltage (V_{out}) = 325 V, switching frequency (f_S) = 25 kHz, average output power (P_{out})= 1 kW.

The on-state resistors of the power switches ($R_{ON,S}$) were considered equal to 0.028 Ω which indicates the internal resistance of NVHL020N120SC1 switch. In contrast, the power switches used in a previous power converter design ([43]) were IGBT power switches without body diodes, which limit the current to flow in only one direction.

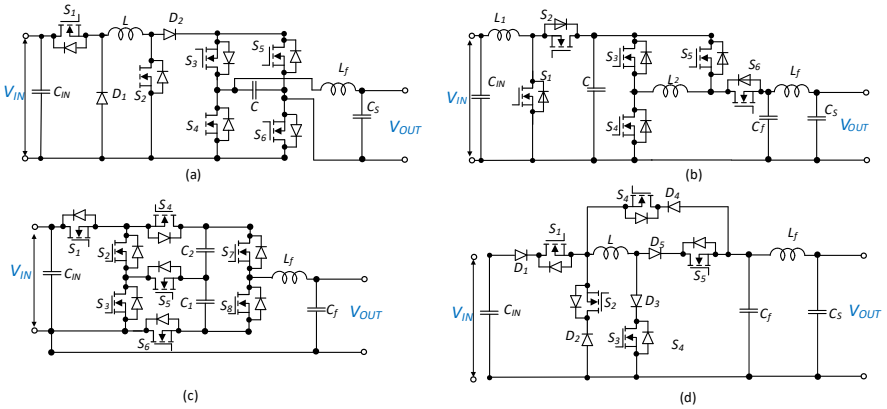


Figure 3.8 Schematics of the compared topologies: (a) buck–boost and the unfolding circuit in [40], (b) flying inductor power converter in [41], (c) switched-capacitor power converter in [42], and (d) flying inductor power converter in [43].

MOSFETs, on the other hand, have bidirectional current flow capability inherently. To account for the unidirectional current flow in the IGBT-based design, a diode was added in series with the power switch in the simulation. For power diodes, the on-state resistance ($R_{ON,D}$) was assumed to be 0.05 Ω, and the forward voltage ($V_{fw,D}$) was assumed to be 0.65 V in the circuit models.

This switch is a N-channel MOSFET power switch with the body diode. In the flying inductor based converter in [43], IGBT power switches without body diodes are used. This causes unidirectional current flowing through the switches, while MOSFETs obtain the inherent bidirectional current flowing capability. Therefore, a diode is connected in series with the power switch in the simulation environment to model the current unidirectional semiconductor for the introduced topology in [43]. The on-state resistors of the power diodes ($R_{ON,D}$) and the forward voltage of power diodes ($V_{fw,D}$) were considered as 0.05 Ω and 0.65 V, respectively for the structures with power diodes.

The comparison between different circuit designs is focused on several key factors, including the accumulated energy of capacitors (WC), the accumulated energy of inductors (WL), the Total Standing Voltage (TSV) of the semiconductors, conduction losses of the semiconductors (PCON), and the number of power switches used (NSW).

Fig. 3.9 presents a radar chart comparing the different circuit topologies based on their calculated parameters shown in per unit values. The inverter introduced in reference [42] uses a switched-capacitor circuit and has the highest capacitor value among the compared designs, resulting in high accumulated energy in the capacitors. However, this topology also has significant conduction losses. Switched-capacitor circuits are susceptible to current spikes that occur when the capacitors are being charged,

causing inrush currents to pass through the power switches in the charging path, leading to higher current stress and power losses. As the output power increases, the magnitude of these current spikes becomes higher, potentially damaging the power switches. Therefore, SC-based solutions are not suitable for high-power applications. The flying inductor converter in [43] has the highest value of conduction losses due to power losses across the series-connected power diodes with the power switches. In contrast, the presented inverter, and the buck–boost unfolding circuit in [40] have the lowest accumulated energy in the capacitors. The introduced power converter in [43] use flying inductor architecture, and the filter capacitor is the only capacitor used in their configuration. The dual-purpose converter in [40] and the presented inverter use a pseudo DC-link approach, which significantly reduces the capacitor size while maintaining good grid current quality. In terms of accumulated energy inside the inductors, the selected dual-purpose power converter stands out among the compared topologies, while the FI-based power converter introduced in [43] ranks highest. Regarding TSV, the introduced flying inductor dual-purpose converter in [41] has the highest voltage stress across its power switches.

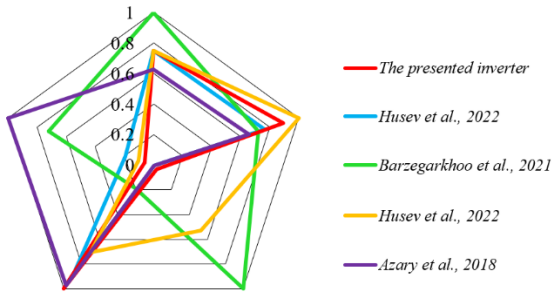


Figure 3.9 Radar chart of the compared topologies.

3.4 Summary

The exploration of various grounding techniques and inverter topologies underscores the critical role of effective leakage current suppression and system safety in power electronic systems, particularly in dc microgrids. Capacitive grounding methods offer simplicity and cost-effectiveness, while high-frequency transformers provide efficient isolation and compactness, albeit with potential EMI concerns. Common-mode chokes offer noise reduction but at the expense of added cost and size. Low-frequency transformers excel in reliability and high-power applications but may pose challenges in space-constrained environments. A common-ground structure emerges as a key strategy to mitigate leakage currents, ensuring stable grounding and minimizing EMI. A common-ground three-level inverter is proposed. A comparative analysis was performed between several common-ground inverters. The comparison methodology was described comprehensively, and the results were shown in the format of a radar chart. It is demonstrated that proposed solution is considered as the best solution among common-ground architectures and is suitable for leakage current suppression in power converters, and in dc system. The presented fault-tolerant inverter continues to work in full power when one of the legs or one of the switches fails. Overall, this section contributes to advancing the understanding of effective grounding techniques and fault-tolerant inverter topologies in dc microgrid systems, paving the way for enhanced efficiency, reliability, and safety in future power electronic applications.

4 Design and analysis of reliable solid-state circuit breakers with increased safety

DC microgrids are becoming increasingly popular due to their high efficiency, universality, and potential application market. However, the reliable protection of these systems still remains a challenge. Circuit breakers as essential components of electrical systems in homes, industrial facilities, and electrical grids ensure the safety of people and electrical equipment. However, fault current interrupting operations in a dc system are significantly more difficult than in an ac system due to the absence of a zero-crossing point in the current as well as the high rate of rise of the fault current. Therefore, the availability of dc circuit breakers becomes crucial, making it a key technology for dc systems.

There are three types of dc circuit breakers: electromechanical, hybrid, and solid-state. Electromechanical breakers do not typically meet the interruption speed requirements for protecting semi-conductor based systems. They also create arcs resulting in the breaker contacts wear out over time, thus increasing the maintenance costs. Using power electronic switches, however, faults can be isolated quickly without creating arcs. As a viable alternative, the hybrid approach combines mechanical and solid-state technologies. Although mechanical disconnectors are employed in these dc circuit breakers, they slow down the current breaking process and increase weight, volume, and investment costs [44]. With the development of power electronic switches in recent years, dc SSCBs have fared much better than mechanical and hybrid circuit breakers due to their high speed and long lifetime. Table 4.1 summarizes the merits and drawbacks of each type of SSCB.

Table 4.1 . Summary of advantages and disadvantages of different circuit breakers [45].

Type		Advantages	Disadvantages
Mechanical circuit breaker		1. Very low power loss 2. Relatively low cost 3. Simple structure	1. Long operating times (30–100 mS) 2. Limited interruption of current capability
Solid-State circuit breaker	Thyristor Based SSCB	1. Automatic tripping for critical fault 2. Lower cost than SSCB with fully controlled switches 3. Reasonable operation speed	1. Fault magnitude needs to be higher for tripping 2. Cannot provide prolonged protection 3. No common ground
	Fully Controlled Switches SSCB	1. Ultra-fast operation (<100 μS) 2. Very long interruption lifetime	1. High power loss 2. Relatively expensive 3. Big size due to heatsink
Hybrid circuit breaker		1. Low power losses 2. No arcing on mechanical contacts 3. Reasonable response time (few mS)	1. Complex technology 2. Current commutation relies on the arc voltage 3. Very expensive

To enhance the fault protection of dc systems, SSCBs have been developed to perform fast protection (<10 µS). However, there are still challenges to address, such as the decoupling of the source and load during operation, the use of switches on the main path, the reliability of MOVs, and the charging of capacitors prior to reclosing. In this section, a soft turn-on auxiliary is first designed to prevent a surge of current due to a capacitance difference between the source and load, and then three bidirectional dc SSCBs are proposed that address the above issues by bypassing the fault current using a third switch. These circuit breakers eliminate the snubber from the power line and do not use the main path switches. These structures also benefit from extra reliability and increased voltage utilization rate of the switches. These features increase both device and human safety.

4.1 Solid-state circuit breaker with soft-reclosing capability

As shown in Fig. 4.1, this topology consists of two MOSFETs back-to-back with an RCD snubber for each MOSFET. As soon as the circuit reaches almost zero current, a mechanical switch turns off the connection between the negative terminals and the input and output terminals. Traditionally, only the positive terminal of a bidirectional SSCB with two switches is disconnected. In addition to increasing safety, the mechanical switch suppresses system disturbances when using more than one SSCB [28].

Fig. 4.1 also represents auxiliary circuitry for the driver of MOSFETs in energy router applications that may encounter voltage differences between the source and load, facilitating the turn-on process. A voltage difference usually occurs between the input and output voltage terminals after the fault is cleared, especially in applications involving energy routers with multiple power sources connected to the dc link. Transient currents can be generated by this voltage difference, which can activate the SSCB. To prevent this, the turn-on process should be as smooth as possible.

An auxiliary circuit for switches is used to resolve the problem mentioned above. As shown in Fig. 4.2(a), it is assumed that there is a voltage difference between V_{dc} and V_O. Considering the gate-source voltage of the MOSFET as shown in Fig. 4.2 (b), an RC circuit is needed for soft turn-on, as demonstrated in Fig. 4.2 (c). By solving the first-order equation of the RC circuit, it is possible to find the gate-source voltage (V_{GS}):

$$V_{GS} = V_K\left(1 - e^{\frac{-t}{RC}}\right), \qquad (4-1)$$

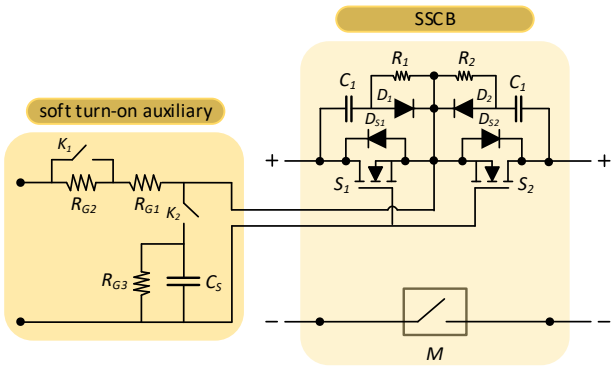


Figure 4.1 Structure of the designed dc SSCB with its soft turn-on auxiliary.

Where, V_K is the voltage of the gate driver. The value of t is the minimum amount of time needed for the circuit voltages to equalize. As a result, it depends on the capacitance of the inputs and outputs and the resistance of the line.

$$t = 5RC. \qquad (4-2)$$

The minimum gate-source voltage (V_{GS}) that can turn on the MOSFET can be obtained by testing a MOSFET or using the datasheet.

The value of *RC* can be calculated by placing V_{GS} and t in Eq. (4-1). For soft turn-on, it seems the easiest solution is to place a capacitor in parallel with the gate-source of the MOSFET and a resistor in series with it. Adding a capacitor, however, will also delay the turn-off process. As a result, it is necessary to place a huge resistor in series with the gate terminal and turn-off resistor R_{G1} and in parallel with a diode so as to not influence the turn-off time (Fig. 4.3(a)). Another structure is to place the diode and resistor in series with each other and in parallel with the turn-off resistor R_{G1} (Fig. 4.3(b)).

However, the aforementioned solution severely affects the gate driver's performance. Therefore, the most complete approach is using the structure in Fig. 4.3(c). In turn-off mode, the mechanical relay K_1 is ON, and relay K_2 is OFF. This means that only the resistor R_{G1} is in the gate auxiliary circuit. On the other hand, in turn-on mode, the state of the relays K_1 and K_2 is reversed and they get OFF and ON respectively which puts the calculated RC in the gate auxiliary circuit. In this circuit, the resistor R_{G3} is in parallel with capacitor to discharge the capacitor for the next turn-on.

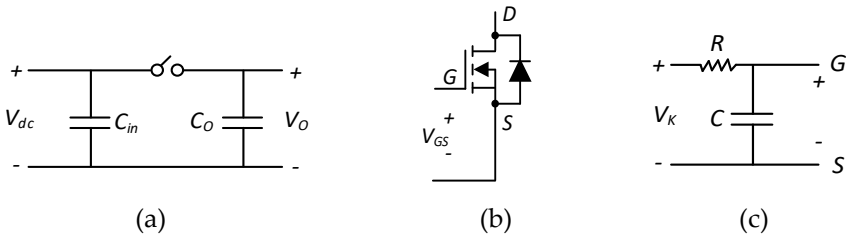


Figure 4.2 Circuits for calculation of the optimized values of R and C: (a) The system with its capacitors of input and output, (b) The gate-source voltage of MOSFET, (c) The auxiliary circuit for the gate of the MOSFET.

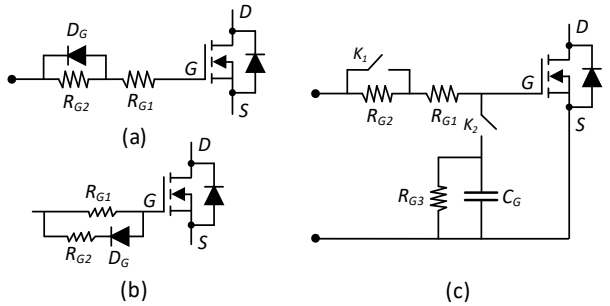


Figure 4.3 The MOSFET and its possible auxiliary circuits: (a) Series approach, (b) Parallel approach, (c) The main and complete approach.

4.2 Solid-state circuit breakers with enhanced safety

The schematics of the proposed SSCBs are shown in Fig. 4.4. These topologies are named according to their shapes like alphabetical letters. Therefore, they are named T-SSCB (Fig. 4.4(a)), Y-SSCB (Fig. 4.4(b)), and H-SSCB Fig. 4.4(c). All three circuits consist of three switches. In addition, T-SSCB is composed of 2 diodes and an RC+MOV snubber, Y-SSCB is composed of 4 diodes and an RC+MOV snubber and Y-SSCB is composed of 4 diodes and two RC+MOV snubbers.

The operating modes of the designed SSCBs are shown in Fig. 4.5. In normal operation, the current flows through both MOSFETs as shown in Figs. 4(a, c, and e). When the short-circuit fault occurs, the third MOSFET S_3 turns on. After a safe delay, the MOSFETs S_1 and S_2 turn off. Therefore, the current of the line inductor is bypassed through the switch S_3 and the snubber as shown in Figs. 4.5(b, d, and f). It should be noted that in T-SSCB, the switches S_1 and S_2 are connected in a different direction from the other two topologies. The MOSFET S_1 is permanently turned off, and the current flows through its diode. It is turned ON when the system works in backward mode.

The proposed SSCBs address the problems of traditional SSCBs making the following contributions:

- Complete decoupling of the primary side with the load side during the interruption ensures the faulty section is quickly and effectively isolated from the fault current to increase safety, reliability and of the load.
- The snubber is removed from the power line, therefore, the MOV's reliability is increased.
- Voltage utilization rate of the switches is increased by 20 %, therefore maximum allowable dc bus voltage on the SSCB is extended.
- Not using switches of the main path which increase reliability.
- Complete and fast discharging of the snubber capacitor before reclosing.
- The SSCB adds the benefits by only adding two diodes and one MOSFET with a low maximum voltage.

The three proposed SSCBs have modularity capabilities that allow them to be easily extended to suit different dc system requirements. The Y-SSCB and H-SSCB, however, would be more suitable for modularization since in T-SSCB, half of the switches are turned ON, decreasing their reliability.

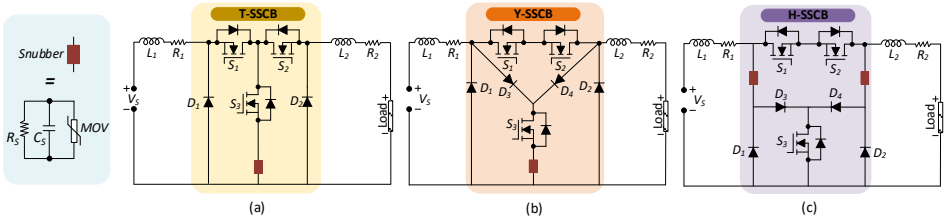


Figure 4.4 The schematics of the proposed SSCBs: (a) T-SSCB (b) Y-SSCB (c) H-SSCB.

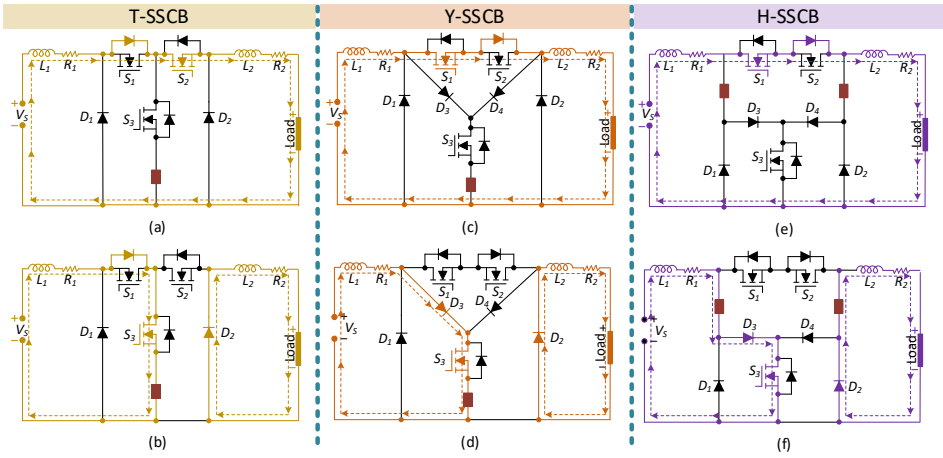


Figure 4.5 Operating modes of the proposed SSCBs: (a) normal operation of T-SSCB, (b) short-circuit operation of T-SSCB, (c) normal operation of Y-SSCB, (d) short-circuit operation of Y-SSCB, (e) normal operation of H-SSCB, (f) short-circuit operation of H-SSCB.

Circuit breakers with high efficiency demonstrate decreased power losses and require less cooling during consistent operating states. One solution to achieve high efficiency in SSCBs is to connect multiple solid-state switches in parallel. This method helps improve overall efficiency by lowering the input switch's equivalent on-state resistance. In accordance with the design parameters of the prototype, the efficiency of the proposed circuit breakers is 99.91 calculated by Eq. (4-3).

$$\mu_{SSCB} = \left(1 - \frac{R_{ds(on)} \cdot I_{dc}}{\mu_V \cdot V_{dc}}\right) \cdot 100\%. \qquad (4-3)$$

As shown in Fig. 4.6, the efficiency of the SSCBs decreases as the nominal current or the on-state resistance of the switches increase. $V_{dc} = 350$ V is used as a reference voltage for the efficiency calculation. When applied in high voltage, the efficiency increases significantly since it is directly proportional to the voltage.

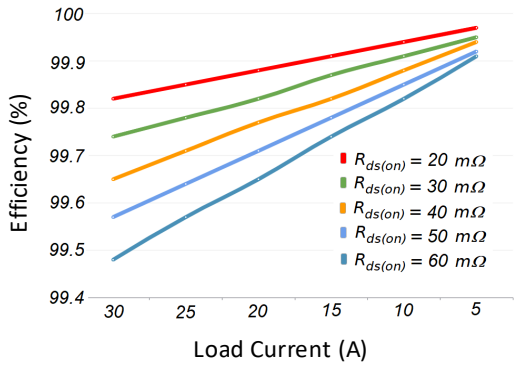


Figure 4.6 The efficiency of the proposed SSCBs for different on-state resistances and currents.

Since solid-state switches are not restricted in terms of their on/off cycles, the lifespan of the breakers is primarily determined by their topology and their operation during the fault isolation procedure. During the isolation process of the proposed SSCBs, no current passes through the switches of the main path which increases their lifetime and reliability reducing their thermal and electrical stress [4].

Since dc systems have low inertia and short circuit fault currents rise rapidly, SSCBs must react quickly to abnormal currents. There are two time intervals included in the response time of an SSCB: detection time and reaction time. The reaction interval is defined as the time between when the fault is detected and when the line current in the system starts to decay.

The proposed SSCBs benefit from high reliability and increased voltage utilization rate of switches of the main path. In most SSCBs with a MOV in parallel with the switches, the voltage of the MOV is equal to the input voltage when the switch is off. As a result, reliability problems arise due to MOV degradation. MOVs suffer degradation as surge currents increase in number and duration, increasing leakage current and decreasing time to failure. Additionally, higher temperatures directly influence the leakage current in MOVs, making it proportional to temperature. MOVs that experience thermal runaway, exceeding their capability, eventually fail due to short circuits [46].

To solve MOV degradation in SSCBs, [47] suggests that V_{dc} should be 20 percent less than the maximum allowable dc voltage on MOV in a steady state. Nevertheless, it gives rise to dimensioning challenges and, more importantly, decreases the main thyristor's voltage utilization rate (μ_V) of the switch which is defined as the following equation.

$$\mu_V = \frac{V_{dc}}{V_{rating,Switch}}.100\%. \qquad (4-4)$$

In the proposed SSCBs, because of the absence of the MOV in the power line, the maximum allowable dc bus voltage on SSCBs and the voltage utilization rate of switches is increased to at least 20%, resulting in improved efficiency due to Eq. (4-3).

Additionally, it increases power density by extending V_{dc} and reducing the number of series-connected switches in MVDC and HVDC applications, as well as enhancing compactness by decreasing cooling systems because it uses lower switches [48].

4.2.1 Operating zones

Fig. 4.7 presents the electrical waveforms of the proposed SSCBs. There are 10 zones determined by the crucial moments of the interruption process. These zones are discussed independently, and the equations of the currents and voltages are given along with the calculations of time intervals.

Zone I (Before t_0): The first zone includes the normal mode when the switches S_1 and S_2 are turned ON. The current flows from the dc source through the circuit breaker to feed the load as shown in Figs. 4.5 (a, c, and e). As shown in Fig. 4.7, during this interval, the voltages of the capacitor(s) and the main switches are zero and the voltage of the third switch equals the dc voltage. The input side current i_{L1} and the output side current i_{L2} are equal to the nominal value I_N:

$$i_{L1} = i_{L2} = I_N = \frac{V_{dc}}{R_{Load}}. \qquad (4-5)$$

Zone II ($t_0 - t_1$): At t_0 short-circuit fault occurs at the output terminals of the system which makes the current of the circuit increase dramatically making the inductors appear in the voltage loop as following equation:

$$(L_1+L_2)\frac{di_L}{dt} - V_{dc} = 0. \quad (4-6)$$

By solving the above first-order differential equation with initial values: $i_{L1}(t=0) = I_N$, the current is calculated as follows:

$$i_{L1} = i_{L2} = \frac{V_{dc}t}{L_1+L_2} + I_N. \quad (4-7)$$

The current at which the fault must be detected is set to I_{limit} in the microcontroller. At t_1 the fault is detected and by approximating the current during T_{0-1} to be linear, the interval $T_{0-1}$is calculated:

$$T_{0-1} = \frac{(L_1+L_2)(I_{Limit} - I_N)}{V_{dc}}. \quad (4-8)$$

Zone III ($t_1 - t_2$): Due to the delay of the microcontroller and current sensor, the SSCB acts at t_2 instead of t_1. By considering T_D as the delay time and assuming $t_0 = 0$, the SSCB's action time T_{0-2} is calculated as follows:

$$t_2 = T_{0-2} = T_{0-1} + T_D. \quad (4-9)$$

By calculating T_D and consequently T_{0-2} by Eq. (4-9), the maximum current of the switches is obtained by Eq. (4-7) as follows:

$$I_P = \frac{V_{dc}T_{0-2}}{L_1+L_2} + I_N. \quad (4-10)$$

Zone IV ($t_2 - t_3$): A safe delay T_S is considered in the control program to prevent S_1 and S_2 from turn-off before turning ON S_3, since the high voltage resulting from the inductor's decreasing current will burn the switch(s).

$$t_3 = t_2 + T_S. \quad (4-11)$$

Because of the delay T_S, there is a difference between the maximum currents of the input and the output side. However, since it is negligible, we consider this approximation:

$$I_P = i_{L1max} \approx i_{L2max}. \quad (4-12)$$

Zone V ($t_3 - t_4$) (at input side): S_1 and S_2 turn OFF (For T-SSCB, S_1 is already turned OFF) and the current of the input inductor commutates to S_3 and the snubber. This current charges the snubber capacitor till its voltage reaches the clamping voltage of MOV, V_{Clamp}. During this interval, the following equations can be derived:

$$L\frac{di_{L1}}{dt} + +R_1 i_{L1} + v_C - V_{dc} = 0. \quad (4-13)$$

$$i_{L1} = C\frac{dv_C}{dt} + \frac{v_C}{R_S}. \quad (4-14)$$

A portion of the inductor's current flows through the snubber resistor, however, its value (v_C/R_S) is negligible in comparison with the current of the snubber capacitor (Cdv_C/dt). By considering this assumption and the initial values $i_L(0) = I_P$ and $v_C(0) = 0$, the voltage of the capacitor can be obtained:

$$v_C = e^{-\alpha t}\left(\left(\frac{I_P}{C_S} + \alpha V_{dc}\right)\frac{\sin(\omega_d t)}{\omega_d} - V_{dc}\cos(\omega_d t)\right) + V_{dc} \quad (4-15)$$

Where, α, ω_0 and ω_d are defined as follows:

$$\alpha = \frac{R_1}{2L_1}, \omega_0 = \frac{1}{\sqrt{L_1 C_S}}, \omega_d = \sqrt{\alpha^2 - {\omega_0}^2}. \quad (4-16)$$

The interval T_{3-4} can be calculated by placing $v_C = V_{clamp}$ and an approximation by considering t→0:

$$T_{3-4} \approx \frac{V_{clamp} C_S}{I_P}. \quad (4-17)$$

Therefore, the time that the input side current reaches zero is obtained as follows:

$$t_4 = t_3 + T_{3-4}. \quad (4-18)$$

Zone VI ($t_4 - t_6$) (at input side): The current commutates to MOV at t_4. By approximating the current in this interval to be linear, the input current is calculated as follows:

$$i_{L1} = I_P - \frac{V_{Clamp} - V_{dc}}{L_1} t. \quad (4-19)$$

By considering $i_1 = 0$, the time interval T_{4-6} and consequently t_6 are calculated:

$$T_{4-6} = \frac{L_1 I_P}{V_{Clamp} - V_{dc}}. \quad (4-20)$$

$$t_6 = t_4 + T_{4-6}. \quad (4-21)$$

Zone VII ($t_3 - t_5$) (at output side): At the output side, the current of the output inductor flows through the diode D_2 to reach zero at t_5. Considering the initial value $i_{L2}(0) = I_P$, for T-SSCB and Y-SSCB, we have:

$$L_2 \frac{di_{L2}}{dt} + R_2 i_{L2} = 0. \quad (1-22)$$

Therefore, the current of the output side inductor can be obtained as follows:

$$i_{L2} = e^{-\frac{R_2 t}{L_2}} I_P. \quad (4-23)$$

The time that the output current reaches zero is obtained:

$$T_{3-5} = 5\zeta. \quad (4-24)$$

Where $\zeta = \frac{L}{R}$.

In the case of H-SSCB:

$$L_2 \frac{di_{L2}}{dt} + R_2 i_{L2} + v_C = 0. \quad (4-25)$$

$$i_{L2} = C \frac{dv_C}{dt} + \frac{v_C}{R_S}. \quad (4-26)$$

Therefore, the current of the load sideline inductor can be obtained by:

$$i_{L2} = -\alpha e^{-\alpha t} \left(\frac{I_P}{C_S} + \alpha V_{dc}\right) \frac{\sin(\omega_d t)}{\omega_d} + e^{-\alpha t} \left(\frac{I_P}{C_S} + \alpha V_{dc}\right) \cos(\omega_d t). \quad (4-27)$$

By considering i_{L2} =0 and an approximation by considering t→0, the time when the output current reaches zero (T_{3-5}) and consequently t_5 is obtained as follows:

$$T_{3-5} \approx \frac{2L}{R_2}. \quad (4-28)$$

$$t_5 = t_3 + T_{3-5}. \quad (4-29)$$

Zone VIII ($t_6 - t_7$): At t_6, when the current of the input side reaches zero, the voltage on the capacitor equals the input dc voltage as well as the voltage on the switch S_1 (the switch S_2 for T-SSCB).

When both currents of the input side and the output side reach zero, the switch S_3 turns OFF after a safe delay $T_Z = T_{6-7}$.

Zone VII ($t_7 - t_8$): At t_7, S_3 turns OFF and the snubber capacitor starts discharging. As the voltage of the capacitor decays to zero, the voltage of the switch S_3 increases to reach V_{dc}. This is because the resistance value across S_3 at the OFF state (Mega range) is much higher than the resistance value of R_S (KΩ range). During this interval, the voltage of the capacitor which has been charged to V_{dc}, discharges to R_S during T_{7-8}:

$$T_{7-8} = R_S C_S. \quad (4-30)$$

Zone IX ($After\ t_8$): At t_8, all components and their voltage and current waveforms return to their normal state before the fault and the interruption is completed, and the converter is ready to restart.

$$t_8 = T_{7-8} + t_Z. \quad (4-31)$$

4.2.2 Design procedure

Table 4.2 summarizes the dependency of each time interval to the value of different parameters of the topologies.

The proper values of snubber capacitance and MOV highly affect the performance of SSCB along with time intervals. Therefore, their appropriate design is of high importance.

Snubber Capacitor, C_S: Considering $v_C(t_4) = V_{clamp}$ in Eq. (4-15), we have:

$$V_{Clamp} = e^{-\alpha T_{3-4}}\left(\left(\frac{I_P}{C_S} + \alpha V_{dc}\right)\frac{\sin(\omega_d T_{3-4})}{\omega_d} - V_{dc}\cos(\omega_d T_{3-4})\right) + V_{dc}. \quad (4-32)$$

By considering t→0, the following approximations can be made to simplify the complex equation:

$e^{-\alpha T_{3-4}} \approx 1$, $\frac{I_P}{C_S} \gg \alpha V_{dc}$, $\sin(\omega_d T_{3-4}) \approx \omega_d T_{3-4}$, $\mathrm{Cos}(\omega_d T_{3-4}) \approx 1$.

Doing so, the value of the snubber capacitor can be derived from Eq. (4-32):

$$C_S \approx \frac{T_{3-4} I_P}{V_{clamp}}. \quad (4-33)$$

By replacing I_P with Eq. (4-10) we obtain the following statement:

$$C_S \approx \frac{T_{3-4}}{V_{clamp}}\left(\frac{T_{0-2} V_{dc}}{L_1 + L_2} + I_N\right). \quad (4-34)$$

Since T_{0-2} has a large dependency on the speed of the microcontroller and the current sensor, L_1+L_2 are line parameters, V_{dc} and I_N are constant and predefined, and also V_{clamp} has its own limit, C_S can be optimized mainly by T_{3-4}.

Snubber Varistor, MOV: The desired MOV can be selected considering three parameters including V_{clamp}, E_r, and I_{Surge}.

The maximum clamp dc voltage V_{clamp} for T-SSCB and Y-SSCB must be 10% lower than the maximum surge voltage of the switches.

$$V_{clamp} < 1.1 V_{S,max}. \quad (4-35)$$

For H-SSCB:

$$V_{clamp} < 2.2 V_{S,max}. \quad (4-36)$$

On the other hand, it also must be 10% higher than $V_{dc,}$;

$$V_{clamp} > 1.1V_{dc}. \quad (4-37)$$

The maximum surge current must be less than the current of the input side inductor at t_4. Hence, according to (14),

$$I_{Surge} < I_P - \frac{V_{MOV} - V_{dc}}{L_1} t_4. \quad (4-38)$$

The surge energy on the MOV during T_{4-6} can be calculated as follows using the derived i_{L1} from Eq. (4-19):

$$E_{surge} = \int_{t_4}^{t_6} V_{MOV} i_{L1} dt \approx$$

$$\int_{t_4}^{t_6} (\frac{V_{dc} - V_{Clamp}}{\mathrm{t}} + V_{Clamp})(I_P - \frac{V_{Clamp} - V_{dc}}{L_1} t). \quad (4-39)$$

The obtained result is the minimum value of surge energy of the MOV:

$$E_{MOV} > E_{surge}. \quad (4-40)$$

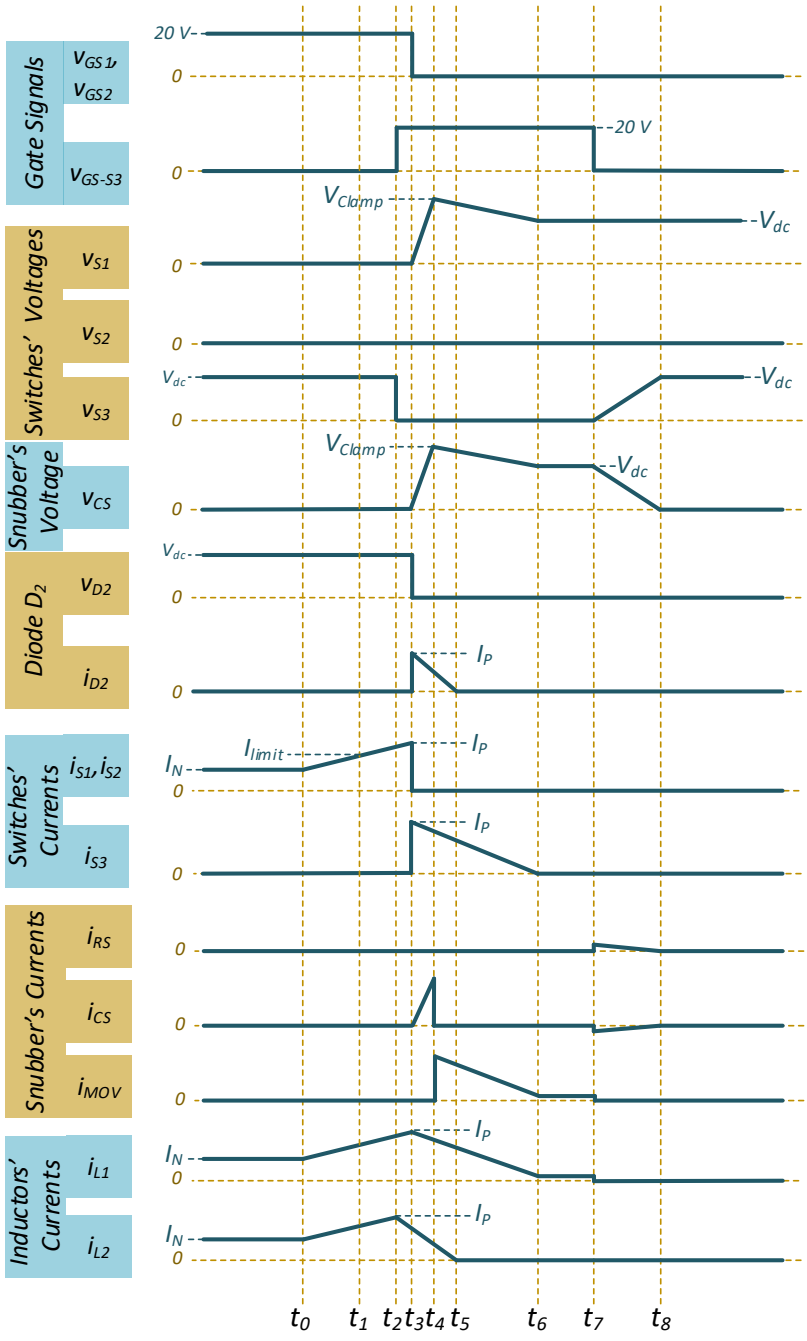


Figure 4.7 Electrical waveforms of the proposed SSCBs.

Table 4.2. Dependency of time intervals to the value of different parameters of the circuit (▲direct relation, ▼inverse relation).

Time Interval	Key Dependencies
T_{0-1}	L_1 ▲ L_2 ▲, I_{Limit} ▲
T_{1-2} (T_D)	The delay of the microcontroller and ▲ The delay of the current sensor ▲
T_{2-3} (T_S)	Chosen by us
T_{3-4}	C_S ▲,V_{clamp}, ▲ I_P ▼
T_{4-6}	L_1 ▲, I_P ▲, V_{MOV} ▼
T_{3-5}	L_2 ▲, R_2 ▼
T_{6-7} (T_Z)	Chosen by us
T_{7-8}	R_S ▲, C_S ▲

4.3 Experimental results

4.3.1 Experimental results of SSCBs with soft-reclosing capability

Fig. 4.8 shows the schematic of the circuits used for the experiment along with the prototype. In the first experiment (Fig. 4.8(a)), the short-circuit is created using a mechanical relay K across the load. Fig. 4.8(c) shows the prototype of the laboratory prototype and test operation of the designed SSCB. The voltage of the dc source is 240 V with a 30 A limit for the circuit's current. The result is shown in Fig. 4.9. The SSCB breaks the circuit after 16µS when the current reaches 100 A and the voltage of the switch S_1 reaches 420 V. As discussed before there is a time delay that depends on the current sensor and the speed of the microcontroller programming. The delay time of the current sensor used in this prototype is 14 µS and the delay of the programming equals the sampling period which is 5 µS. These delays do not sum up since they occur simultaneously. This time delay can be reduced using a current sensor with a larger bandwidth.

However, after reducing it to the sampling period, to further decrease the delay, the sampling frequency should be increased. However, as discussed in the previous section it raises the peak voltage of the switch during fault-clearing operation so there should be a lower limit for the delay according to the components' capability.

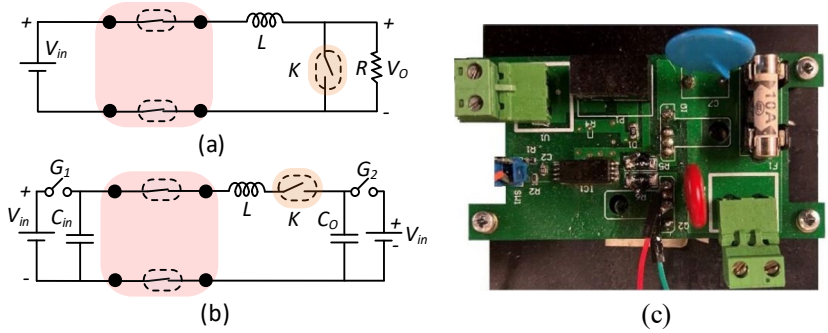


Figure 4.8 Experimental results of the soft turn-on test: V_{dc} =400 V, V_{out} =350 V.

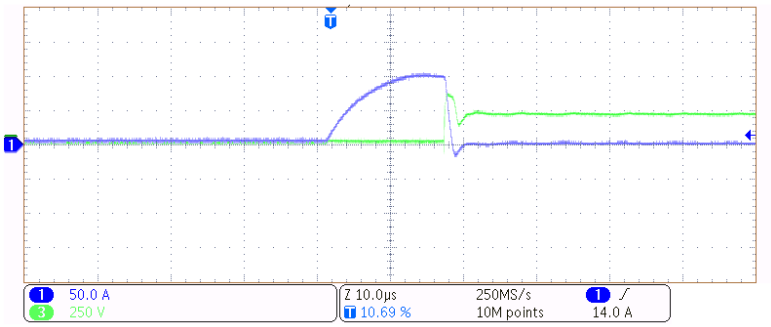


Figure 4.9 Experimental results of the short-circuit test: V_{in} =240 V, I_{limit} =30 A.

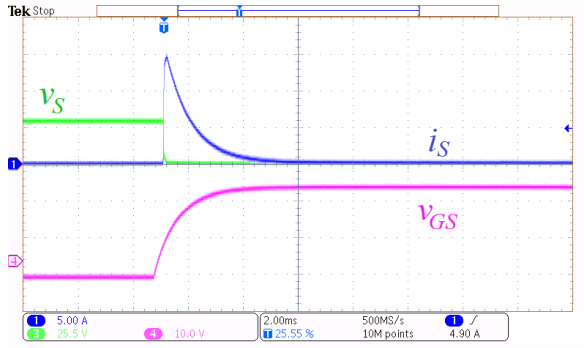


Figure 4.10 Experimental results of the soft turn-on test: V_{dc} =401 V, V_{out} =350 V.

In the second test as shown in Fig. 4.8(b), the main path of the circuit is connected through a mechanical switch. The capacitors are charged to different voltages by turning on the switches G_1 and G_2 temporarily. Then, by disconnecting these switches and connecting switch K, there will be a huge current spike because of the input and output capacitors' voltage difference dropped on the small resistance of the circuit.

As shown in Fig. 4.10, there is a 50 V voltage difference between the input and output capacitors which by the benefit of using a 10 kΩ resistor and a 100 nF capacitor as mentioned before, the peak of the surge current is limited to is 25 A which is very desirable.

4.3.2 Experimental results of SSCBs with increased safety

Fig. 4.11(a) shows the schematic of the test circuit of the prototypes and the laboratory prototype of the designed SSCBs is presented in Fig. 4.11(b). In this test, the short-circuit is created using a mechanical relay K across the load. Two inductors are placed in the input and output terminal of the SSCB as line inductors with values 10µH and 20µH, respectively. The input dc voltage is 500 V, and the output resistor is 50 Ω as the load. The complete list of the design parameters is presented in Table 4.3.

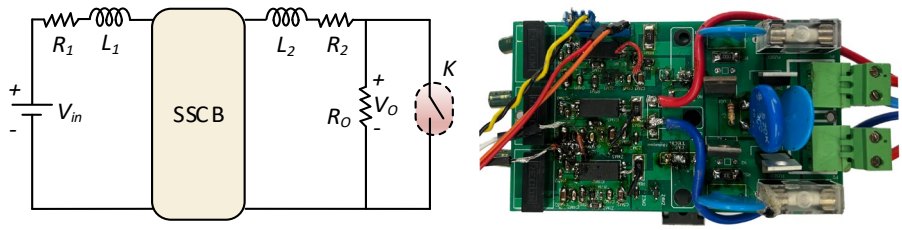


Figure 4.11 (a)Schematic of the test circuit. (b) The prototype of the SSCB.

Table 4.3. Design parameters of the proposed SSCBs.

Parameter	Acronym	Value
Rated Power	P	12.5 kW
Input Voltage	V_{in}	500 V
Nominal current	i_N	25 A
MOSFETs	S_1, S_2, S_3	UF3SC120016K4S
Diodes	D_1, D_2, D_3, D_4	APT30DQ120KG
Snubber Resistor	R_S	3KΩ
Snubber Capacitor	C_S	500nF, 2kV
Snubber MOV	MOV	V_{dc} =505 V, V_{Clamp}: 1000 V
Input side Inductor	L_{Line}	10 µH
Output side Inductor	L_{Out}	20 µH
Load Resistor	R_{Load}	50 Ω
Input side Resistor	R_1	1.5 Ω
Output side Resistor	R_2	1.5 Ω

The input voltage is 500 V, and the nominal current is 25 A. Using a 505 V MOV with clamping voltage of 1000 V, the overvoltage on the switches is 950 as shown in Fig. 4.12(a). Fig. 4.12(b) shows the output side current that reaches its peak at 180 A and decays to zero in 21 µS. The voltage experiences an oscillation when the third switch turns off. This oscillation depends on the safe delay T_S. As shown in Figs. 4.12(c) and 4.12(e), the peak short circuit current in this test in the input side is 195 A while the limit current to be detected is set to 100 A. The overcurrent is detected and reacts in 9 µS. After the detection and reaction, the current reaches 180 A. Following this, the switch S_3 turns on which makes a short circuit across the input side and bypasses the short circuit current into the third leg. To protect the switches, the switch S_2 is turned off after a short time interval T_S which is considered 1 µS here. During this 1 µS, the short current passes through a closer path to the source and sees a lower resistance, therefore the current increases with a sharper pace until it reaches its peak when the input current starts to plummet. In T-SSCB, the maximum voltage peak voltage of the snubber capacitor and therefore the switch S_2 equals the maximum clamping voltage of MOV. It takes 47 µS for i_{L2} and 24 µS for i_{L1} to reach zero. When the input current i_{L1} reaches the MOV's leakage value, after a safe interval of 5 µS the switch S_3 turns off to completely make it zero.

In Y-SSCB, the input current passes through the diode D_3. Also, unlike T-SSCB, the source pins of the switches are connected instead of the drains that places the voltage stress on the switch S_1. The results in this case are similar to T-SSCB, however, the current does not pass through any of the power line switches.

H-SSCB has an extra snubber in series with its output side diode making it benefit from faster fault clearance in the load side which is about 5 µS in this test (Fig. 4.12(c)). However, since there is a reverse voltage on the output side snubber capacitor, the voltage of the drain pin of MOSFET S_2 is $-V_{Clamp}$. Therefore, the voltage across the switch S_1 will be $2V_{Clamp}$. This structure is suitable in applications where fast fault clearance is needed on both sides and where cost is not a priority and switches with higher voltage can be used.

Figs. 4.12(d) and 4.12(e) show the current of the capacitor rising at the time of breaking operation and commutating to MOV when the voltage of the switch S2 reaches near the clamping voltage.

The 9 µS reaction time depends on the speed of the microcontroller's program along with the delay of the current sensor. The current implemented current sensor is ACS720KLATR-15AB-T, which has an 8 µS delay. By using a high bandwidth current sensor, the detection time can be decreased considerably.

Fig. 4.13 compares the voltage of the snubber capacitor in the steady state in the proposed SSCB and a typical conventional SSCB in Fig. 4.1. Unlike the traditional approach, the capacitor in the proposed SSCB is discharged before reclosing. According to Eq. (4-30), the discharging time depends on the value of the snubber resistor.

By analyzing the voltage of the switches in the proposed SSCB and the conventional one in Fig. 4.14, it is seen that using the same MOV, using a higher dc input voltage is possible in the proposed SSCBs and in general in the SSCBs in which MOV is removed from the power line. In traditional SSCBs with MOV in their power line, the input voltage must be at least 20% higher than MOV's voltage to avoid leakage currents.

It is illustrated from the experimental results that the proposed SSCBs can work properly in different voltage levels below the clamping voltage of the MOV with a safe margin which is attractive for industrial applications.

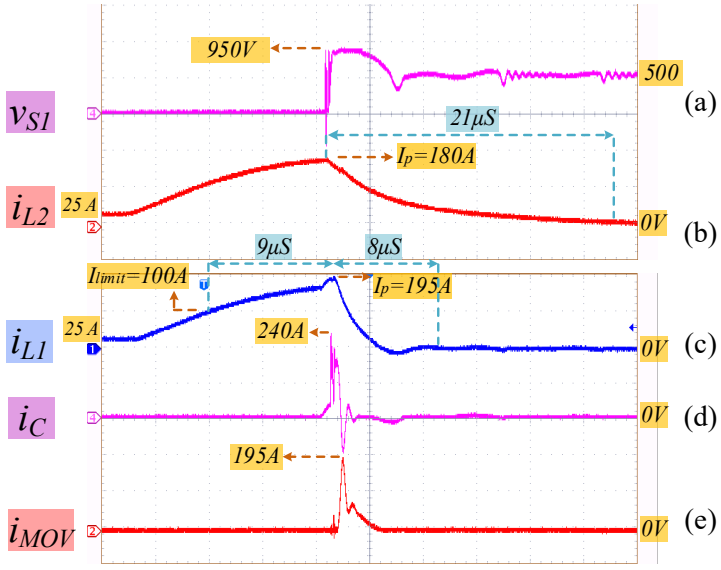


Figure 4.12 The electrical waveforms of Y-SSCB.

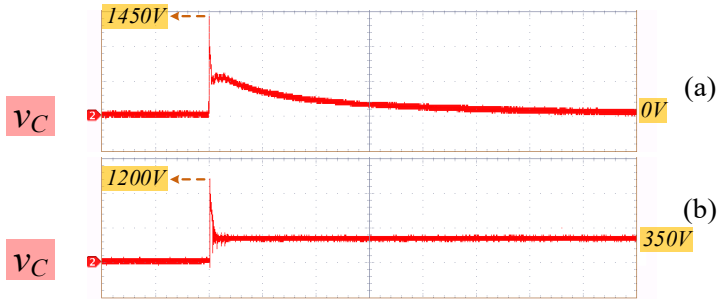


Figure 4.13 The voltage of snubber capacitor in: (a) Proposed SSCBs, (b) Conventional SSCB in Fig. 4.1.

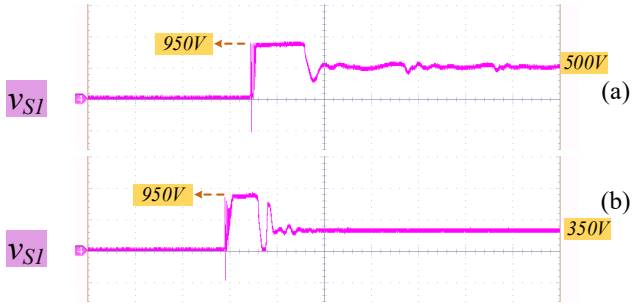


Figure 4.14 The overshot voltage on the switches: (a) Proposed SSCBs, (b) Conventional SSCB in Fig. 4.1.

4.4 Summary

The development and analysis of reliable Solid-State Circuit Breakers (SSCBs) for dc microgrids offer significant advancements in fault protection and safety. The proposed SSCBs, featuring a soft turn-on auxiliary circuit, address key challenges such as decoupling the source and load, enhancing MOV reliability, and managing charged capacitors during reclosing. Three innovative SSCB topologies (T-SSCB, Y-SSCB, and H-SSCB) are designed with a third switch to bypass fault currents, eliminating snubbers from power lines and increasing voltage utilization rates. These designs improve reliability, efficiency, and safety while reducing component count and costs. The optimized auxiliary circuit ensures soft turn-on, preventing high current surges and voltage overshoots, thus extending the lifespan and reliability of the circuit breakers. The experimental results validate the effectiveness of these SSCBs, demonstrating their potential for increased safety and efficiency in dc microgrids.

The findings of this section support the first hypothesis, which states that advanced solid-state circuit breakers provide completely safe operation of the energy router in case of a fault.

5 Energy router for residential applications

The integration of renewable energy sources in buildings and smart houses is pivotal for advancing sustainable living and combating climate change. In addition, the reduction of cost of renewable energy sources has opened new opportunity for the consumers to produce their own electricity [49]. In smart houses, energy routers play a critical role by optimizing the distribution and usage of renewable energy, enhancing energy efficiency, and ensuring that power is utilized where and when it is needed most. This intelligent energy management not only lowers utility costs for homeowners but also contributes to a more resilient and eco-friendly energy grid, making it key for future urban planning and protecting the environment.

The designed energy router is an intelligent power electronic equipment that enables using both ac and dc in residential buildings. It manages the energy transfer between photovoltaic dc sources, energy storage systems, three-phase ac sources, dc, and ac loads [50]. The device also typically includes advanced power management function to ensure stable and reliable energy distribution. Additionally, the power electronic energy router includes communication capabilities for remote monitoring and control, as well as a built-in protection mechanism to safeguard against electrical faults or overloads.

The smart energy router harnesses the power of a three-phase ac source for enhanced stability and avoids overloading, ensuring the longevity of electrical components. It efficiently distributes energy across single-phase structures and intelligently chooses the optimal phase based on time and consumption patterns and maximizes efficiency by aligning energy distribution with demand. It also results in a considerable reduction of the primary cost of the PV and battery systems.

In this chapter, after the description of the energy router's topology along with its power management structure, the Printed Board Circuit (PCB) design considerations of the prototype are explained. The energy router consists of a three-level inverter and two dc-dc converters which are described with experimental results.

5.1 Topology description

The structure of this energy router consists of a bidirectional single-phase inverter to act as interface between the ac grid and the dc link. It also includes a dc-dc converter to use dc power provided by PV panels on the house's rooftops. To store the dc power at moments when PV panels cannot provide enough power, a battery is used by connecting an unfolding dc converter to the dc link.

A standout feature of this energy router lies in its common-grounded structure, meticulously designed to suppress leakage currents, and elevate safety standards. Within this framework, the novel solid-state circuit breaker in this structure exhibits the ability to isolate both the source and load sides entirely. This remarkable characteristic not only enhances device safety but also prioritizes human safety. The PCB layout of the energy router is implemented with high level EMC design.

The contributions of the designed energy router structure are:

- Selection of state-of-the-art power electronic converters and circuit breaker to ensure optimal and reliable performance.
- Merging of conventional smart house functions along with intelligent energy control.

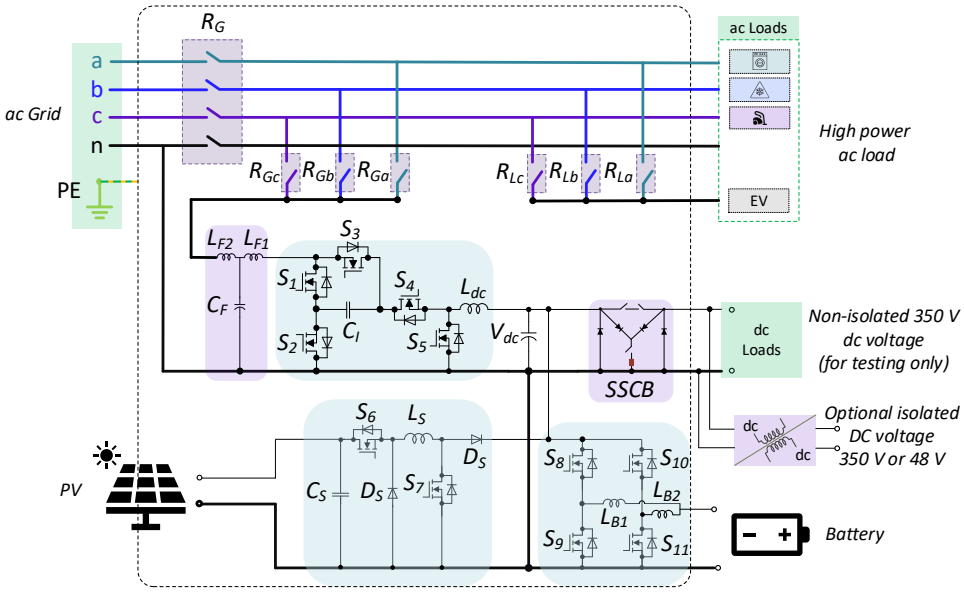


Figure 5.1 Schematic of the energy router.

- Common-grounded structure which eliminates the leakage current and increases the safety.
- High efficiency for dc sources and loads.
- Enhanced Protection functions including a novel SSCB with enhanced safety.
- High scalability for grid extension.
- Active and reactive power control for ac grid.

5.2 Power management structure

The ac port of the energy router features three phases, each intricately connected to an ac load within the house through a dedicated relay for every phase. Within this system, three ac loads operate simultaneously, and at any given moment, the Electric Vehicle (EV) charger port is selectively linked to the ac load with the least power consumption.

To elaborate, each ac load is linked to the ac side of the inverter through a relay. However, only one ac load is actively connected to the inverter at any specific moment, the one exhibiting the highest power consumption among the three ac loads. This entails a dynamic system where the ac load with the highest power demand is supplied by the dc sources through the inverter, facilitated by activating the corresponding relay.

Concurrently, the two remaining ac loads, which exhibit lower power consumption, are supplied by the ac grid. This is achieved by activating the relays corresponding to the respective phases of the ac grid. This intricate arrangement optimizes energy distribution within the household, considering that all three ac loads typically do not operate at their maximum power capacity simultaneously.

Essentially, this method ensures that the dc side, comprising the Photovoltaic system and the battery, only needs to supply one-third of the household's ac loads—the major power consumers at any given time. The remaining power requirement is seamlessly met by the ac grid. Consequently, the capacity of the dc side, inclusive of the PV system and the battery, is effectively reduced to one-third, promoting an efficient and balanced

energy utilization strategy within the household. To govern the operation of the energy router, high-level algorithms are needed to monitor the input from the three-phase source, analyze the power requirements of the connected single-phase loads, and turn on the relays accordingly. This ensures that the single-phase loads receive a consistent and reliable power supply and is out of scope of this work.

5.3 Prototype description

The PCB design of the energy router in both 2D and 3D forms is presented in Figs. 5.2(a) and 5.2(b), respectively. During the design of the four-layer PCB for the energy router, which integrates both the control board and power board, several crucial considerations were implemented to ensure optimal performance and minimize EMI. The forward path and return path were aligned on different layers, with the signal trace placed on the top layer and its corresponding return path directly underneath the adjacent ground plane. This arrangement minimized the loop area, significantly reducing EMI.

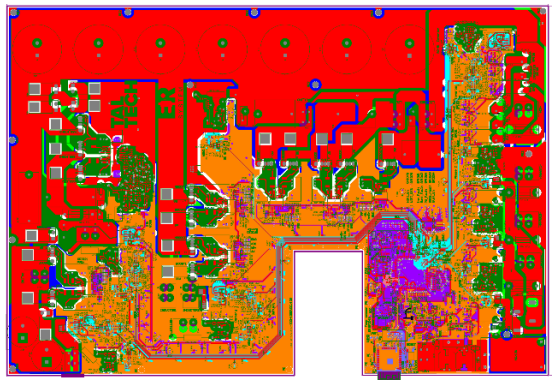


Figure 5.2 PCB design of the energy router in 2D from.

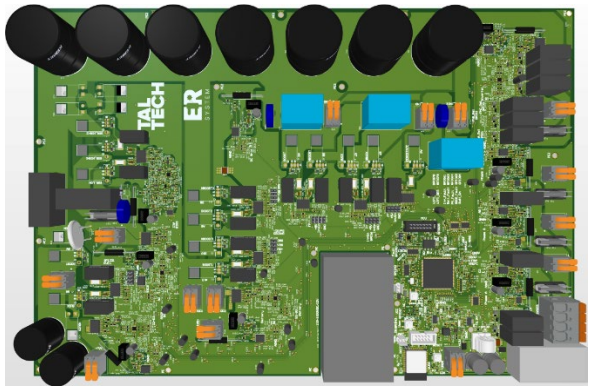


Figure 5.3 PCB design of the energy router in 3D form.

Analog and digital grounds were carefully separated to prevent noise from digital circuits affecting the analogue components. These grounds were connected at a single point using star grounding to avoid ground loops and maintain a common reference point. To maintain power integrity, one inner layer was dedicated as a continuous power plane, providing a stable and clean power supply to all components. Decoupling capacitors were placed close to the power pins of integrated circuits, filtering high-frequency noise, and stabilizing the power supply.

Component layout was meticulously planned to separate high-frequency components from sensitive analogue parts, reducing potential interference. Critical signal traces were kept as short as possible and routed away from noisy areas. Differential pairs were routed together to maintain signal integrity and reduce EMI, with controlled impedance traces designed for high-speed signals to prevent signal degradation.

Thermal management was another key consideration. For the power board section, which handles higher currents, thicker copper layers were used to dissipate heat effectively. Thermal vias were strategically placed to transfer heat from the top layer to the inner and bottom layers, ensuring even thermal distribution. Power components were arranged to avoid heat concentration, promoting efficient thermal management.

Ground fills and copper pours were used extensively around signal traces to provide extra shielding and further reduce EMI. These ground fills also aided in heat dissipation. For high-speed and high-frequency signals, adjacent ground planes were positioned to act as shields, minimizing radiated emissions and improving signal integrity. Through these detailed considerations, the PCB design for the energy router achieved a balance of performance, reliability, and EMI compliance, ensuring robust operation across various conditions.

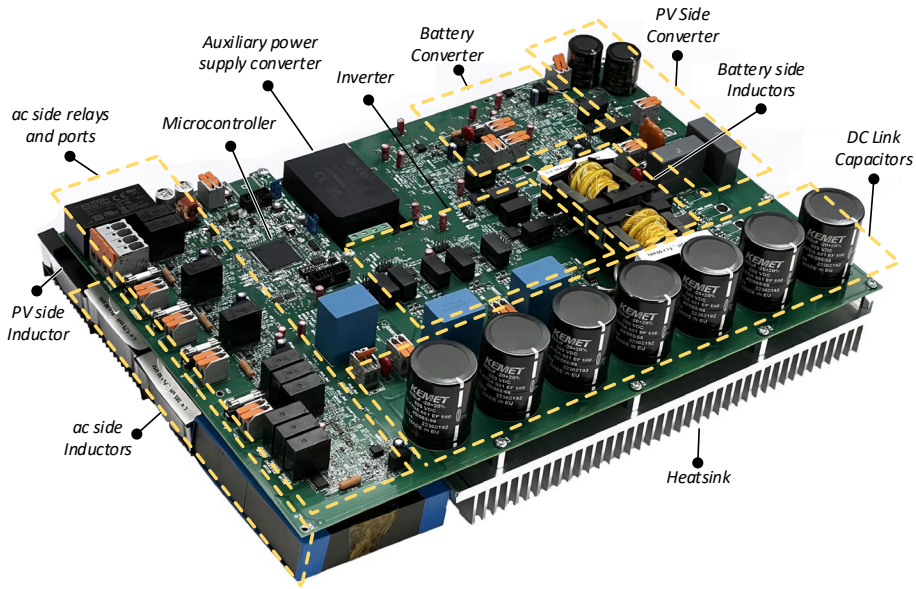


Figure 5.4 The prototype of the energy router assembled in the power electronics lab of TalTech.

Table 5.1. Design parameters of the energy router.

Parameter	Acronym	Value
Rated Power	P	15 kW
Grid and load side ac voltage (RMS)	V_{in}	230 V, 50 Hz
DC link voltage	V_{DC}	350 V
Nominal current of each phase	i_N	25 A
Switching frequency	f_{in}	65 kHz
Solar voltage input range	V_S	150 – 600 V
Battery input voltage range	V_B	150 – 330 V
Power switches of inverter	$S_1 \dots S_5$	C3M0025065K
Power switches of dc-dc converters	$S_6 \dots S_{11}$	C3M0021120K
Dc link capacitor	C_{dc}	3 mF
Inductor of inverter	L_{dc}	1.8 mH
Flying capacitor of inverter	C_I	3 µF
Filter inductors of inverter	L_{F1}, L_{F2}	680 µH, 320 µH
Filter capacitor of inverter	C_F	3.3 µF
Microcontroller	-	TMS320F28379D
Gate Driver	-	UCC21521CDW
Relays	$R_G, R_{Ga}, R_{Gb}, R_{Gc}, R_{La}, R_{Lb}, R_{Lc}$	G5PZ-1A4-E_DC12
Capacitor of buck-boost converter	C_S	100 µF
Inductor of buck-boost converter	L_S	850 µH
Diode of buck-boost converter	D_S	IDH20G120C5XKSA1
Inductors of boost converter	L_{B1}, L_{B2}	500 µH

5.4 Experimental results

The laboratory test prototype of the energy router is demonstrated in Fig. 5.4. The design parameters of the designed energy router are outlined in Table 5-1. The rated power of the device is 15 kW while the ac voltage on both the grid and load sides is 230 volts at 50 Hz. The dc link voltage is set at 350 V and a high switching frequency of 65 kHz ensures efficient energy conversion and control. The solar voltage input range spans from 150 to 600 V, accommodating various photovoltaic panel configurations and environmental conditions. Similarly, the battery input voltage range is specified as 150 V to 330 V, allowing for flexibility in battery selection and integration.

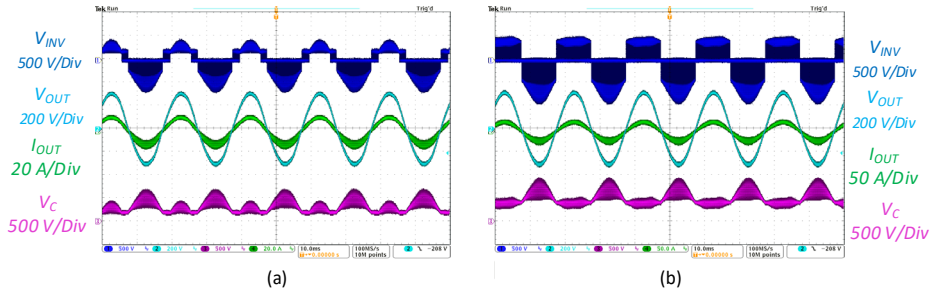


Figure 5.5 Experimental results of the inverter: (a), V_{in} = 200 V, P_{OUT} =2 kW, (b): V_{in} = 400 V, P_{OUT} =3.5 kW.

5.4.1 The three-level Inverter

The operation of the energy router's inverter is described in section 3. Here, the experimental results of the three-level common-ground inverter are demonstrated and explained. Measurements were conducted using Tektronix TPA-BNC voltage probes, TCP0150 current probes, and MDO4034B-3 digital oscilloscopes.

Fig. 5.5 shows the operation of the inverter including the output voltage before filtering (V_{INV}), the output voltage after filtering (V_{OUT}), the output current (I_{OUT}) and the voltage across the capacitor (V_C). 325 V is considered as the nominal peak value of the output voltage.

The results in Fig. 5.5(a) are obtained under 200 V input voltage. It is seen that V_{INV} is a three-level waveform which confirms the successful operation of the power converter in boost mode. Also, it is shown that V_{OUT} is a sinusoidal 50 Hz waveform, and its peak value reaches 325 V. Regarding the 200 V input voltage, this result confirms that the topology steps up the output voltage successfully. In this figure, I_{OUT} is a sinusoidal 50 Hz waveform and its peak value equals to approximately 12 A which corresponds to nearly 2 kW output power. It is also in phase with V_{OUT}, as expected under resistive load. In this figure, the voltage stress across the capacitor is shown.

The indicated results in Fig. 5.5(b) are obtained under 400 V input voltage. It is seen that V_{INV} is a three-level waveform with the highest value of 325 V. It confirms the successful operation of the power converter in buck mode. The peak value of I_{OUT} is approximately 22 A which corresponds to 3.5 kW output power.

Fig. 5.6 is devoted to the efficiency study of the converter without auxiliary power supply losses. Two output power levels are considered including 2 kW under V_{in}=200 V, and 3.6 kW under V_{in}=400 V. It is seen that the efficiency reaches approximately 97.8 % at 0.7 kW when the input voltage is fed by 200 V. The efficiency reaches 97.8 % at 1.5 kW under V_{in}=400 V. It is included from these figures that the highest efficiency is 97.8 %. It is also evident that maximum powers are not the same under V_{in}=200 V and V_{in}=400V. On one hand, the input current is limited by saturation current of the inductor, on the other hand, in case of boost operation, the losses are higher and in order to keep the same maximum dissipative power, the input power has to be cut. It is very common for most industrial converters, in particular in the solar industry.

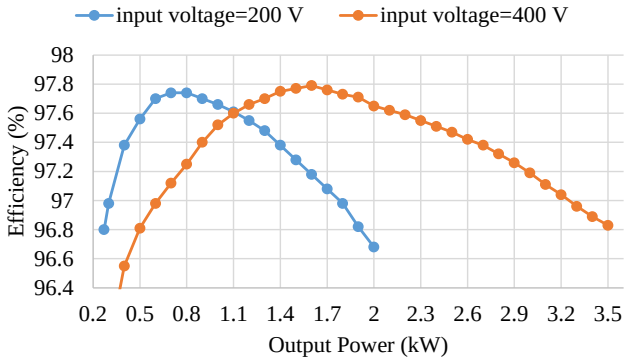


Figure 5.6 Efficiency study of the common-ground converter in different power levels.

5.4.2 The buck-boost dc-dc converter

In the designed energy router, a buck-boost dc-dc converter is used to stabilize and optimize the variable dc voltage generated by the panel, which fluctuates due to changing sunlight conditions. The converter ensures a consistent output voltage suitable for powering devices or charging batteries.

The experimental results for one operation point are demonstrated in Fig. 5.6. As demonstrated in this figure, the input and output currents are approximately 15 A and 8 A, while the voltages of the input and output are 200 V and 350 V respectively. Maximum efficiency approached 99 %.

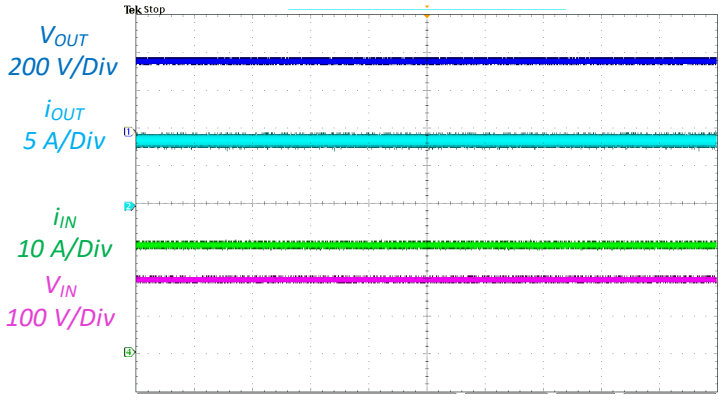


Figure 5.7 Experimental results of the buck-boost dc-dc converter.

5.4.3 The interleaved dc-dc converter

An interleaved boost dc-dc converter is connected directly to a battery in the energy router to precisely manage the charging and discharging processes, ensuring that the battery operates within safe voltage and current limits. It is comprised of four switches and two inductors. By interleaving two phases, the frequency of the output current ripple is effectively doubled. This reduction in the output current ripple is crucial for maintaining the health and longevity of the battery, as lower ripple currents decrease the thermal and electrical stress on the battery cells. Furthermore, the interleaved design allows for current sharing between two phases, reducing conduction losses. This improvement in efficiency is particularly beneficial in battery-connected systems where minimizing power losses is critical to extending battery life and improving overall system performance.

Examples of the experimental results of the interleaved boost converter are demonstrated in Fig. 5.7. As demonstrated in this figure, the input current is approximately 20 A, the output current is half this value at about 12 A. The voltages of the input and output are 200 V and 350 V respectively, which approves the boost capability of the converter. The current ripple is very small on the input side, while it is negligible at the output side. Maximum efficiency was higher than 98 %.

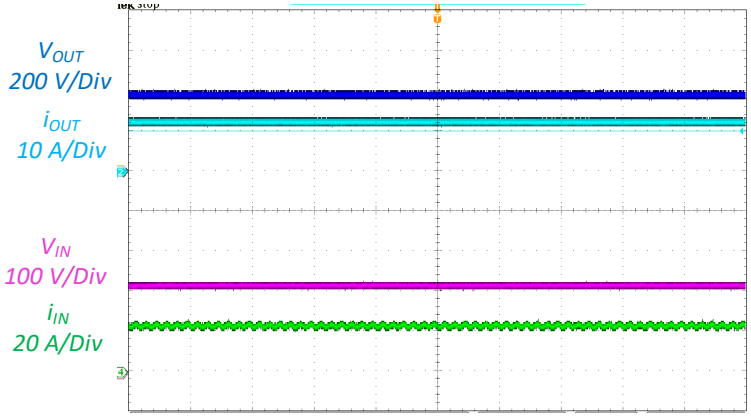


Figure 5.8 Experimental results of the interleaved boost dc-dc converter.

5.5 Summary

The designed energy router facilitates the use of both ac and dc power within a household and enhances energy management within residential buildings. It manages energy flow between PV, dc sources, energy storage systems, three-phase ac grid, and both dc and ac loads. The energy router's common-grounded structure is designed to suppress leakage currents and enhance safety, while the novel solid-state circuit breaker implemented within the structure provides complete decoupling of source and load sides during the fault clearance. The PCB layout is optimized for high-level EMC design. Through meticulous experimentation and analysis, the chapter demonstrates the practical viability of the converters implemented in the proposed energy router, showcasing its ability to manage the power efficiently.

This section approves the second hypothesis that common-ground interface solves the leakage current issue with no isolation requirements. During the experimental verification there is not any leakage current detected thought dc or ac systems.

Also, the context of this section indirectly approves the fourth hypothesis that single-phase power electronic interface with smart internal relays and energy management algorithm is sufficient to balance three-phase single-family house supply system.

6 Conclusions

The research undertaken in this thesis first, explores lifetime management techniques and fault-tolerant converters. By conducting a thorough analysis of lifetime extension methods and fault-tolerant designs, the research highlights the importance of these strategies in enhancing the reliability and longevity of power electronic systems. The proposed techniques, including hardware redundancy and switching state redundancy, provide robust solutions for managing faults and extending the operational life of these systems.

Another significant contribution of this work is the investigation and implementation of common-ground structures. This approach effectively addresses the challenge of leakage current suppression, which is critical for ensuring system safety and stability.

The design and analysis of reliable SSCBs form another part of this thesis. The introduction of SSCBs with soft-reclosing capabilities and enhanced safety features represents an innovative advancement in power protection technology. The experimental results demonstrate that these SSCBs improve the safety of power electronic systems by ensuring fast and reliable fault clearance.

An innovative aspect of this research is the development of an energy router specifically designed for residential applications. The designed energy router with a selection of state-of-the-art power electronic converters and a safety-enhanced circuit breaker ensures optimal and reliable performance. This energy router efficiently manages energy flow between ac and dc grids and loads. By monitoring energy usage across three ac phases and selecting the phase with the highest demand to be supplied by dc sources, the system's costs is reduced by only requiring the PV and battery systems to supply one-third of the total household energy at any given time.

The experimental validations conducted in this thesis provide strong evidence of the practical viability and enhanced performance of the proposed systems. The successful implementation and testing of the energy router prototype demonstrate its capability to manage diverse energy sources efficiently, ensuring a seamless integration of renewable energy into residential applications.

In conclusion, this thesis makes significant strides in the development of advanced energy management systems. By addressing key challenges related to lifetime management, fault tolerance, grounding, and protection mechanisms, the research paves the way for more reliable and efficient energy systems. Future work will focus on scaling these innovations to preindustrial prototypes (TRL6-8) and high-level control implementation, aiming to bring these advancements closer to widespread adoption and real-world application. The findings and contributions of this thesis are poised to play a crucial role in shaping the future of sustainable energy management, ultimately contributing to a more resilient and efficient energy infrastructure.

As a results of thesis, the author **claims** the following:

- Reliable design of power electronic systems requires lifetime management techniques including lifetime analysis, lifetime assessment and condition monitoring along with fault management approaches such as hardware redundancy and imbalance control.

  However, since control techniques without redundancy only compensate imbalance in the performance of the converters and cannot fully compensate and clear the fault, the third hypothesis is not relevant to this case. Residential application can not tolerate significant cost increasing.

- The proposed soft turn-on auxiliary circuit can be added to the circuit breakers to achieve soft reclosing capability within the systems that may experience input and output voltage imbalances of up to 50 V.
- The proposed family of dc SSCB completely decouples the input and output terminals during the fault clearance and increases the voltage utilization rate of the switches by 20% while providing a fast protection under 10 µS.

  It validates the first hypothesis that advanced solid-state circuit breakers provide completely safe operation of the energy router in case of a fault.
- The energy router is designed with common-ground non-isolated feature to suppress leakage current. It also decreases the required rated power of PV and battery to one-third. It approves the second hypothesis that common-ground interface solves the leakage current issue with no isolation requirements. This confirms the fourth hypothesis that single-phase power electronic interface with smart internal relays and energy management algorithm is sufficient to balance three-phase single-family house supply system.

List of figures

List of tables

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Abstract
Common-ground energy router structure with enhanced reliability and protection

This thesis introduces a smart energy router for residential applications, focusing on the advancement of power electronics to enhance its reliability and protection. Investigating lifetime management techniques, including the analysis, assessment, and extension of the lifetime of power electronic systems, helps identify potential failure modes, develop strategies to mitigate risks, and optimize the design and operation of these systems. Methods to suppress leakage current in power electronic converters are studied, and a three-level inverter is implemented in the energy router using a common-ground structure to minimize leakage current. After the classification of fault management techniques to enhance the reliability of power converters, a fault-tolerant structure is proposed, which is common-ground, ensuring continuous operation even in the presence of faults.

The thesis introduces novel SSCBs designed for dc microgrids, which incorporate a soft turn-on auxiliary circuit to solve the voltage imbalance of the input and output terminals of power systems at the time of reclosing. Three innovative SSCB topologies (T-SSCB, Y-SSCB, and H-SSCB) are presented, featuring a third switch that bypasses fault currents, thereby eliminating snubbers from power lines and increasing voltage utilization rates. They also address challenges such as decoupling the source and load, improving MOV reliability, and managing charged capacitors during reclosing. These designs improve system reliability, efficiency, and safety while reducing component count and costs. Experimental results validate the effectiveness of the proposed SSCBs, demonstrating their potential for enhanced fault protection and safety in dc microgrids.

Additionally, the thesis introduces a smart energy router for residential applications. This device enables the integration and management of both ac and dc power sources, including photovoltaic systems, energy storage systems, and various loads. The energy router intelligently distributes power across single-phase structures, optimizes phase selection based on time and consumption patterns, and reduces the rated power of photovoltaic and battery systems. Through these innovations, the thesis contributes to the development of more reliable and efficient solutions for modern electrical systems.

Lühikokkuvõte
Ühise nulljuhtmega suurendatud töökindluse ja kaitsega energiaruuter

See töö tutvustab nutikat energiaruuterit eramutele keskendudes jõuelektroonika edendamisele selle usaldusväärsuse ja kaitse suurendamiseks. Elutsükli haldusmeetodite uurimine, sealhulgas jõuelektroonikasüsteemide eluea analüüs, hindamine ja pikendamine, aitab tuvastada potentsiaalseid rikkeid, arendada riskimaandusstrateegiaid ning optimeerida nende süsteemide projekteerimist ja tööd. Uuritakse lekkevoolu summutusmeetodeid jõuelektroonikamuundurites ning energiaruuteris rakendatakse kolmetasemelist inverterit, mis minimeerib lekkevoolu ühise maandusstruktuuri abil. Lisaks rikkehaldusmeetodite klassifitseerimisele muundurite töökindluse tõstmiseks pakutakse välja ühise maandusega riket taluv struktuur, mis tagab pideva töö ka rikkeolukorras.

Doktoritöö tutvustab uuenduslikke alalisvoolu mikrovõrkudele mõeldud pooljuhtkaitselüliteid (SSCBd), mis rakendavad sujuvkäivitusabiahelat, et tasakaalustada sisend- ja väljundterminalide pinged enne taas sisselülitamist. Esitletakse kolm uudset SSCB topoloogiat (T-SSCB, Y-SSCB ja H-SSCB), millel on kolmas lüliti rikkevoolu möödajuhtimiseks, vältides nõnda summutusahelaid toiteliinides ning suurendades pingekasutusmäära. Need käsitlevad ka alalispinge väljakutseid nagu allika ja koormuse lahutamine, metalloksiidvaristori (MOV) usaldusväärsuse parendamine ja laetud kondensaatorite haldamine ahela taassulgumisel. Sellised kaitselülitid parandavad süsteemi usaldusväärsust, tõhusust ja ohutust, vähendades samal ajal komponentide arvu ja kulusid. Katsetulemused kinnitavad pakutud SSCB-de tõhusust, näidates nende potentsiaali alalisvoolu mikrovõrkudes rikkekaitse tõhustamiseks ja ohutuse tagamiseks.

Lisaks tutvustab doktoritöö nutikat energiaruuterit eramutele. See seade võimaldab nii vahelduv- kui ka alalispingeallikate sh päikesepaneelide, energiasalvestussüsteemide ja erinevate koormuste integreerimist ning haldamist. Energiaruuter jaotab nutikalt võimsust faaside vahel, optimeerides faasivalikut aja ja tarbimismustrite põhjal ning maksimeerides efektiivsust, kohandades energia jaotamist nõudlusega. See lähenemine mitte ainult ei paranda stabiilsust ja väldib ülekoormust, vaid vähendab oluliselt ka päikesepaneelide ja akusüsteemide põhikulusid. Nende uuenduste kaudu panustab doktoritöö usaldusväärsemate, tõhusamate ja odavamate kaasaegsete energiahaldussüsteemide arengusse.

Appendix

[PAPER-I] S. Rahimpour, O. Husev, and D. Vinnikov, “A Family of Bidirectional Solid- State Circuit Breakers with Increased Safety in DC Microgrids”, IEEE Transactions on Industrial Electronics.

A Family of Bidirectional Solid-State Circuit Breakers With Increased Safety in DC Microgrids

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***Abstract*—Increasingly, dc microgrids are attracting attention because of their universality, high efficiency, and potential application market. To enhance the fault protection of dc systems, solid-state circuit breakers (SSCBs) have been developed to perform fast protection. However, there are still challenges including decoupling of the source and load during operation, using the switches of the main path, MOV's reliability, and charged capacitors before reclosing. In this article, three bidirectional dc SSCBs are proposed that address the aforementioned issues using a third switch to bypass the fault current, eliminating the snubber from the power line, not using the main path switches, and placing a snubber that provides a discharged capacitor before reclosing. These also provide the structure extra reliability and increased voltage utilization rate of the switches. These features increase both device and human safety. The working principle and operating modes of these SSCBs along with the equations for calculation of crucial time intervals, voltages, and currents and the design procedure are provided, and the experimental results demonstrate the proper performance of the topology and validate the findings.**

***Index Terms*—Bidirectional circuit breaker, circuit breaker, dc protection, solid-state circuit breaker.**

I. Introduction

DC GRIDS have been widely adopted in various applications, from renewable energy sources such as solar energy and wind energy to aircraft propulsion systems [1]. With a dc bus, problems such as harmonic, imbalance, and synchronization issues associated with ac systems are eliminated, leading to a simplified control [2]. Moreover, due to the lack of bulky traditional transformers, a higher power density is possible. As a result, dc microgrids are becoming increasingly popular for onboard power systems [3], [4], [5]. However, the reliable protection of these systems still remains a challenge [6]. Circuit breakers as essential components of electrical systems in homes, industrial facilities, and electrical grids ensure the safety of people and electrical equipment. However, fault current interrupting operations in a dc system are significantly more difficult than in an ac system due to the absence of a zero-crossing point in the current as well as the high rate of rise of the fault current. Therefore, the availability of dc circuit breakers becomes crucial, making it a key technology for dc systems. Numerous dc circuit breaker topologies have been published and patented, which are reviewed in [7] and [8].

Dc circuit breakers can be classified into three types: 1) Electromechanical, 2) hybrid, and 3) solid-state. Typically, electromechanical breakers do not meet the interruption speed requirements to protect semiconductor based. Moreover, they create arcs and as a result of arcing, the breaker contacts wear out over time and increase maintenance costs. [9]. However, it is possible to isolate faults quickly without creating arcs by using power electronic switches. The hybrid approach, which combines mechanical and solid-state technologies, has been accepted as a viable option. Although, the mechanical disconnector employed in these dc circuit breakers decreases power loss, it slows down the current breaking process and increases the weight, volume, and investment cost. In recent years, dc solid-state circuit breakers (SSCBs) have greatly advanced due to the development of power electronic switches, which are extremely faster than mechanical and hybrid circuit breakers in addition to the long lifetime. A summary of merits and drawbacks of each type of SSCB is compiled in Table I.

In another aspect, these SSCBs can be classified into two categories based on whether they use semicontrolled switching devices such as silicon controlled rectifiers (SCRs) or fully controlled switching devices such as insulated-gate bipolar transistor and metal-oxide-semiconductor field-effect transistor (MOSFETS). Impedance-source SSCBs as the most common solutions for using half-controlled switching devices are reviewed in [10]. Compared to full-controlled SSCBs, SCR-based SSCBs benefit from lower conduction losses, higher capacity, and lower cost [11]. However, since SCRs require a reverse voltage to turn OFF, reliably generating a reverse voltage across them during the turn-OFF process is the most important part of designing an SCR-based SSCB. On the other hand, SSCBs with fully

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TABLE I
SUMMARY OF ADVANTAGES AND DISADVANTAGES OF DIFFERENT CIRCUIT BREAKERS [14], [15], [16], [17], [18], [19]

Type		Advantages	Disadvantages
Mechanical circuit breaker		1. Very low power loss 2. Relatively low cost 3. Simple structure	1. Long operating times (30–100 mS) 2. Limited interruption of current capability
Solid-State circuit breaker	Thyristor Based SSCB	1. Automatic tripping for critical fault 2. Lower cost than SSCB with fully controlled switches 3. Reasonable operation speed	1. Fault magnitude needs to be higher for tripping 2. Cannot provide prolonged protection 3. No common ground
	Fully Controlled Switches SSCB	1. Ultra-fast operation (<100 μS) 2. Very long interruption lifetime	1. High power loss 2. Relatively expensive 3. Big size due to heatsink
Hybrid circuit breaker		1. Low power losses 2. No arcing on mechanical contacts 3. Reasonable response time (few mS)	1. Complex technology 2. Current commutation relies on the arc voltage 3. Very expensive

controlled switching devices, have total control over the breaking process [12].

The turn-OFF process of an SSCB generates a high di/dt when a short circuit occurs in a dc system; this inductive energy is applied across main switches due to transmission line inductance and current limiting line inductors, which generates very high dv/dt and overvoltage. This can cause the device to fail due to exceeding its rating voltage along with gate signal oscillation which could lead to false turn-ON. In addition, gate-oxide degradation can also be induced by a high dv/dt causing reliability and lifetime issues [13].

To reduce the rising rate, voltage spike and snubber circuits are required. A variety of snubber configurations for SSCBs are reviewed in [20]. Utilizing a capacitor alone or with metal-oxide varistor (MOV) decreases the overvoltage on switches by getting charged during the breaking operation [21]. However, pure C snubbers or C+MOVs cause oscillation due to the system inductance along with discharging high currents during turn-ON. The discharge current can be dampened using a snubber resistor in series with the capacitor. Using a MOV in parallel with an *RC* snubber will also significantly reduce capacitance requirements. The voltage across the resistor in an *RC* snubber or *RC*+MOV is reflected onto power semiconductors when the switch is turned OFF causing extra voltage stress and power shock. As an alternative, a resistor-capacitor-diode (*RC*D) snubber can be used to separate charging and discharging paths [22]. Zhang and Saeedifard [24] used just a MOV along with increasing gate resistance of the switches to decrease the voltage overshoot. Unlike power electronics converters, increasing the gate resistance will not provide switching loss due to rare turning ON and OFF. However, there should be a tradeoff between voltage overshoot and breaker operation delay (which is equal to the turn-OFF delay.

A typical approach to protect dc systems is using two back-to-back fully controlled semiconductor switches. Fig. 1(a) demonstrates such an SSCB, which utilizes MOV-*RC*D as the snubber of the switches. When a short-circuit fault occurs, the first switch gets turned OFF and the current commutates to the snubber and makes its path through the second switch. Therefore, along with using a switch of the main path, a path will still remain from the source to the load through the snubbers during the interruption and after that. This jeopardizes both human safety and device safety especially when oscillations at output terminals appear. In this SSCB, the snubber capacitor remains charged till the next reclosing.

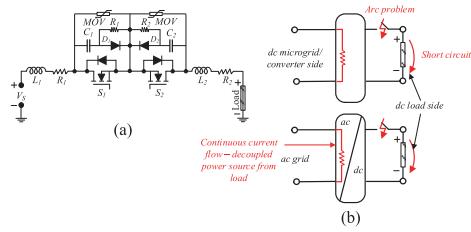

Fig. 1. (a) Typical conventional bidirectional SSCB. (b) Problem illustration.

This conventional solution seems to be not sufficient to provide safe operation for possible applications in the interlink converters between ac and dc grids. From one side, many research works concentrate on isolated solutions, which simplify requirements on SSCB and provide natural dc side fault decoupling from ac side [25], [26]. On another side, there are no standards that define isolation as a strict requirement. Taking into account, that the neutral wire of ac grid and the middle wire of the dc grid should be grounded and so far, connected indirectly, the absence of isolation can be very reasonable. It simplifies power electronics and increases overall efficiency. At the same time, it enhances requirements for dc SSCBs. In the case of a nonisolated dc grid, any fault from the load side has to be decoupled from the dc or ac grid, as illustrated in Fig. 1(b). It shows that despite any fault (open or short circuit) appearing from the dc load side, the source side should be smoothly disconnected mimicking normal operation for a while. It means that some more sophisticated solutions apart from those illustrated in Fig. 1(a) are required.

An MOV degrades as the number and duration of surge currents increase. This occurs when the MOV is in a power line tolerating V_{dc} during the OFF state. Degradation of an MOV increases its leakage current increasing power consumption and temperature. As the MOV heats up, its leakage current keeps rising and finally leads to thermal runaway. Utilizing a thermal fuse in series or using a mechanical switch to disconnect MOV from the power line are the possible solutions but they have major drawbacks. As a solution, using active snubbers to set zero voltage on MOV in the OFF state has been used in recent publications.

The T-type bidirectional circuit breaker proposed in [27], as shown in Fig. 2(a), has a module in the third arm in series with

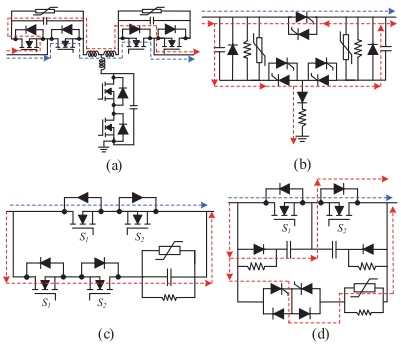

Fig. 2. Some recent proposed bidirectional SSCBs. (a) [27], (b) [28], (c) [30], (d) [30]. Blue arrows show the current during normal mode. Red arrows show current during fault operation.

an inductor to operate as a shunt compensator. The capacitors of are used for both energy absorption during faults, and energy storage during normal operation. Therefore, they are sized larger than the typical snubber circuits. It suffers from a large number of switches, leakage current in the main path, and a lack of complete decoupling of the input and output.

The bidirectional SSCB proposed in [28] and demonstrated in Fig. 2(b), uses six thyristors and two snubber modules. MOVs are disconnected from the power line when SSCB is OFF to solve MOVs' reliability issues [29]. During the interruption, current flows through the lower thyristors, therefore, in this SSCB, the input and output sides are not isolated during breaking. The capacitors in this SSCB are larger than the typical ones since during breaking, one of them needs to be discharged in the other one with a high current to turn OFF the thyristor of the main path and break the circuit.

The SSCB demonstrated in Fig. 2(c) utilizes two back-to-back MOSFETS with an *RC*+MOV snubber [30]. However, the presence of snubber in the circuit is controlled by another set of back-to-back switches in order to eliminate the MOV from the power line, which decreases its degradation and increases the utilization rate of the switches. Using these two extra switches also disconnects the input and output terminals after breaking but not during the breaking process.

To decrease the complexity of control, the proposed SSCB in [30] uses thyristors as the switches of the snubber to turn OFF automatically when its current is lower than the holding current of the thyristors [see Fig. 2(d)]. In this topology, unlike the previous one, decoupling of the input and output terminals is not provided, and it uses the switches of the main path during the fault clearance process.

This article proposes three novel bidirectional circuit breakers that can be used in all dc applications range from renewable energy sources and microgrid to data centers and electric vehicle charging stations. They can be installed at primary busbars providing protection for the entire microgrid, various feeder lines, and near critical load connection points. However, the experimental prototypes in this article are designed with current and voltage characteristics of residential applications specially to use at the dc load side of residential energy routers. In these energy routers, the input voltage of the SSCB is around 350 V and the current is around 25 A.

The proposed SSCBs address the problems of traditional SSCBs making the following contributions.

1) Complete decoupling of the input and output during the interruption and after that, which increases both device and human safety.
2) The snubber is removed from the power line and the main switch so the MOV's leakage current is eliminated and the MOV's reliability and voltage utilization of the switches increases.
3) They do not use the switches of the main path during fault clearance (except T-SSCB), which increases the reliability.
4) Complete and fast discharging of the snubber capacitor before reclosing.
5) Decreased voltage overshoot on the switches.
6) High modularity capability with increased power density due to an increase in the voltage utilization rate of the switches.
7) Benefiting from the abovementioned features at a reasonable cost due to having a small number of components with minimum specifications.

However, these three SSCBs have pros and cons compared to each other, which are discussed further in the article. Calculations and design parameters for these SSCBs are provided in Section II. After that, experimental results are provided to validate the proper performance of all three SSCBs, followed by more discussion in the "discussion" and "conclusion" sections.

II. Proposed Topologies

The schematics of the proposed SSCBs are shown in Fig. 3. These topologies are named according to their shapes similar to alphabetical letters. Therefore, they are named T-SSCB [see Fig. 3(a)], Y-SSCB [see Fig. 3(b)], and H-SSCB Fig. 3(c). All three circuits consist of three switches. In addition, T-SSCB is composed of two diodes and an *RC*+MOV snubber, Y-SSCB is composed of four diodes and an *RC*+MOV snubber and Y-SSCB is composed of four diodes and two *RC*+MOV snubbers.

The operating modes of the designed SSCBs are shown in Fig. 4. In normal operation, the current flows through both MOSFETs, as shown in Fig. 4(a), (c), and (e). When the short-circuit fault occurs, the third MOSFET S_3 turns ON. After a safe delay, the MOSFETs S_1 and S_2 turn OFF. Therefore, the current of the line inductor is bypassed through the switch S_3 and the snubber, as demonstrated in Fig. 4(b), (d), and (f). It should be noted that in T-SSCB, the switches S_1 and S_2 are connected in a different direction from the other two topologies. In this topology, the MOSFET S_1 is permanently turned OFF, and the current flows through its diode. It is turned OFF when the system works in backward mode.

Fig. 5 presents the electrical waveforms of the proposed SSCBs. There are 10 zones determined by the crucial moments of the interruption process. These zones are discussed independently, and the equations of the currents and voltages are given along with the calculations of time intervals.

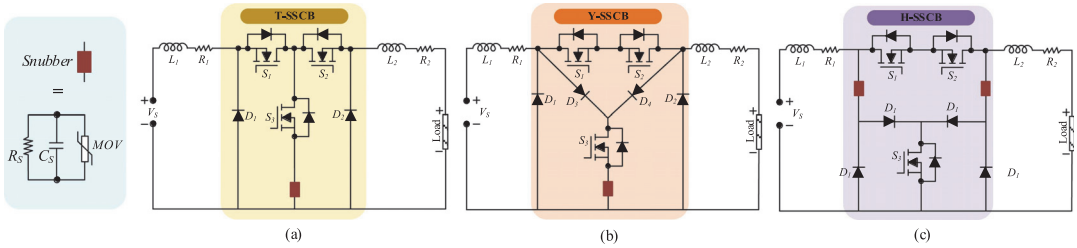

Fig. 3. Schematics of the proposed SSCBs. (a) T-SSCB. (b) Y-SSCB. (c) H-SSCB.

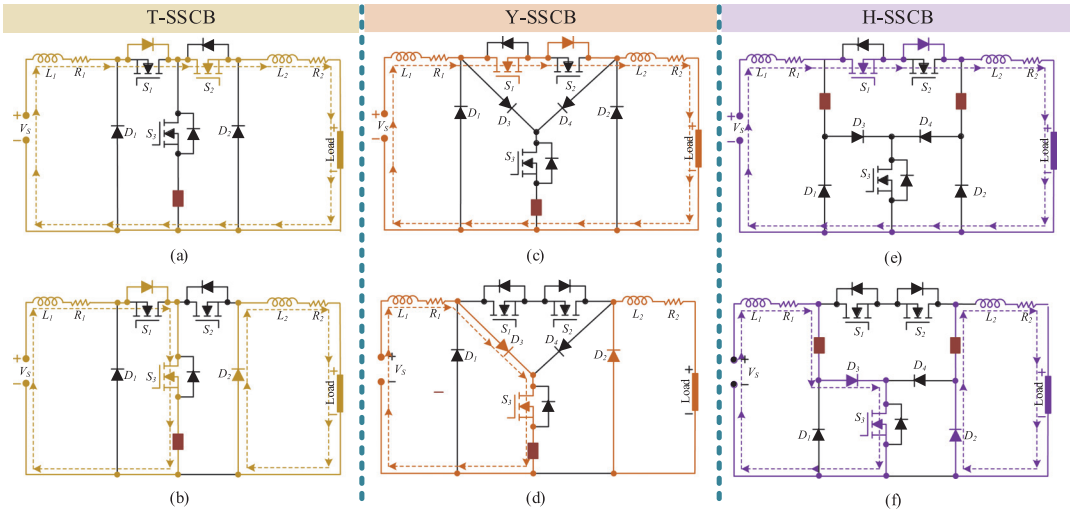

Fig. 4. Operating modes of the proposed SSCBs. (a) Normal operation of T-SSCB. (b) Short-circuit operation of T-SSCB. (c) Normal operation of Y-SSCB. (d) Short-circuit operation of Y-SSCB. (e) Normal operation of H-SSCB. (f) Short-circuit operation of H-SSCB.

Zone I (Before t_0): The first zone includes the normal mode when the switches S_1 and S_2 are turned ON. The current flows from the dc source through the circuit breaker to feed the load, as shown in Fig. 4(a), (c), and (e). As shown in Fig. 5, during this interval, the voltages of the capacitor(s) and the main switches are zero and the voltage of the third switch equal the dc voltage. The input side current i_{L1} and the output side current i_{L2} are equal to the nominal value I_N

$$i_{L1} = i_{L2} = I_N = \frac{V_{\rm dc}}{R_{\rm Load}}. \tag{1}$$

Zone II ($t_0 - t_1$): At t_0 short-circuit fault occurs at the output terminals of the system, which makes the current of the circuit increase dramatically making the inductors appear in the voltage loop as following equation:

$$(L_1 + L_2)\frac{di_L}{dt} - V_{\rm dc} = 0. \tag{2}$$

By solving the abovementioned first-order differential equation with initial values: $i_{L1}(t = 0) = I_N$, the current is calculated as follows:

$$i_{L1} = i_{L2} = \frac{V_{\rm dc}t}{L_1 + L_2} + I_N. \tag{3}$$

The current at which the fault must be detected is set to $I_{\rm limit}$ in the microcontroller. At t_1 the fault is detected and by approximating the current during T_{0-1} to be linear, the interval $T_{0-1}$is calculated

$$T_{0-1} = \frac{(L_1 + L_2)\,(I_{\rm Limit} - I_N)}{V_{\rm dc}}. \tag{4}$$

Zone II ($t_1 - t_2$): Due to the delay of the microcontroller and current sensor, the SSCB acts at t_2 instead of t_1. By considering T_D as the delay time and assuming $t_0 = 0$, the SSCB's action time T_{0-2} is calculated as follows:

$$t_2 = T_{0-2} = T_{0-1} + T_D. \tag{5}$$

By calculating T_D and consequently T_{0-2} by (5), the maximum current of the switches is obtained by (3) as follows:

$$I_P = \frac{V_{\rm dc}T_{0-2}}{L_1 + L_2} + I_N. \tag{6}$$

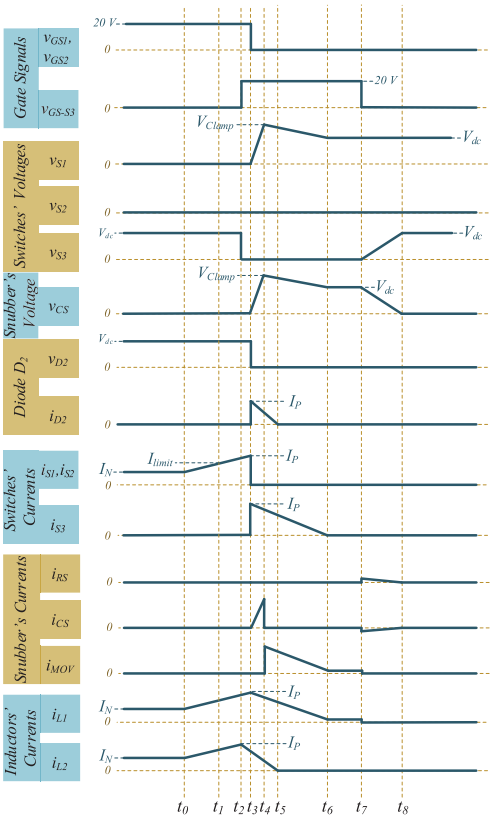

Fig. 5. Electrical waveforms of the proposed SSCBs.

Zone III ($t_2 - t_3$): A safe delay T_S is considered in the control program to prevent S_1 and S_2 from turn-OFF before turning ON S_3, since the high voltage resulting from the inductor's decreasing current will burn the switch(s)

$$t_3 = t_2 + T_S. \tag{7}$$

Because of the delay T_S, there is a difference between the maximum currents of the input and the output side. However, since it is negligible, we consider this approximation

$$I_P = i_{L1\max} \approx i_{L2\max}. \tag{8}$$

Zone IV ($t_3 - t_4$) (at input side): S_1 and S_2 turn OFF (For T-SSCB, S_1 is already turned OFF) and the current of the input inductor commutates to S_3 and the snubber. This current charges the snubber capacitor till its voltage reaches the clamping voltage of MOV, V_{Clamp}. During this interval, the following equations can be derived:

$$L\frac{di_{L1}}{dt} + +R_1 i_{L1} + v_C - V_{\text{dc}} = 0 \tag{9}$$

$$i_{L1} = C\frac{dv_C}{dt} + \frac{v_C}{R_S}. \tag{10}$$

A portion of the inductor's current flows through the snubber resistor, however, its value (v_C/R_S) is negligible in comparison with the current of the snubber capacitor (Cdv_C/dt). By considering this assumption and the initial values $i_L(0) = I_P$ and $v_C(0) = 0$, the voltage of the capacitor can be obtained

$$v_C = e^{-\alpha t}\left(\left(\frac{I_P}{C_S} + \alpha V_{\text{dc}}\right)\frac{\sin(\omega_d t)}{\omega_d} - V_{dc}\cos(\omega_d t)\right) + V_{\text{dc}} \tag{11}$$

where α, ω_0 and ω_d are defined as follows:

$$\alpha = \frac{R_1}{2L_1}\ ,\ \ \omega_0 = \frac{1}{\sqrt{L_1 C_S}}\ ,\ \ \omega_d = \sqrt{\alpha^2 - \omega_0^2}\ . \tag{12}$$

The interval T_{3-4} can be calculated by placing $v_C = V_{\text{clamp}}$ and an approximation by considering t$\rightarrow$0

$$T_{3-4} \approx \frac{V_{\text{clamp}} C_S}{I_P}. \tag{13}$$

Therefore, the time that the input side current reaches zero is obtained as follows:

$$t_4 = t_3 + T_{3-4}. \tag{14}$$

Zone IV ($t_4 - t_6$) (at input side): The current commutates to MOV at t_4. By approximating the current in this interval to be linear, the input current is calculated as follows:

$$i_{L1} = I_P - \frac{V_{\text{Clamp}} - V_{\text{dc}}}{L_1}t. \tag{15}$$

By considering $i_1 = 0$, the time interval T_{4-6} and consequently t_6 are calculated

$$T_{4-6} = \frac{L_1 I_P}{V_{\text{Clamp}} - V_{\text{dc}}} \tag{16}$$

$$t_6 = t_4 + T_{4-6}. \tag{17}$$

Zone V ($t_3 - t_5$) (at output side): At the output side, the current of the output inductor flows through the diode D_2 to reach zero at t_5. Considering the initial value $i_{L2}(0) = I_P$, for T-SSCB and Y-SSCB, we have

$$L_2\frac{di_{L2}}{dt} + R_2 i_{L2} = 0. \tag{18}$$

Therefore, the current of the output side inductor can be obtained as follows:

$$i_{L2} = e^{-\frac{R_2 t}{L_2}} I_P. \tag{19}$$

The time that the output current reaches zero is obtained

$$T_{3-5} = 5\zeta \tag{20}$$

where $\zeta = \frac{L}{R}$.

In the case of H-SSCB

$$L_2\frac{di_{L2}}{dt} + R_2 i_{L2} + v_C = 0 \tag{21}$$

$$i_{L2} = C\frac{dv_C}{dt} + \frac{v_C}{R_S}. \tag{22}$$

TABLE II
DEPENDENCY OF TIME INTERVALS TO THE VALUE OF DIFFERENT PARAMETERS OF THE CIRCUIT (▲ DIRECT RELATION, ▲INVERSE RELATION)

Time Interval	Key Dependencies
T_{0-1}	L_1 ▲ L_2 ▲, I_{Limit} ▲
T_{1-2} (T_D)	The delay of the microcontroller and ▲ The delay of the current sensor ▲
T_{2-3} (T_S)	Chosen by us
T_{3-4}	C_S ▲,V_{clamp}, ▲ I_P ▼
T_{4-6}	L_1 ▲, I_P ▲, V_{MOV} ▼
T_{3-5}	L_2 ▲, R_2 ▼
T_{6-7} (T_Z)	Chosen by us
T_{7-8}	R_S ▲, C_S ▲

Therefore, the current of the load side line inductor can be obtained by

$$i_{L2} = -\alpha e^{-\alpha t}\left(\frac{I_P}{C_S}+\alpha V_{\text{dc}}\right)\frac{\sin(\omega_d t)}{\omega_d} + e^{-\alpha t}\left(\frac{I_P}{C_S}+\alpha V_{\text{dc}}\right)\cos(\omega_d t). \tag{23}$$

By considering $i_{L2}=0$ and an approximation by considering t→0, the time when the output current reaches zero (T_{3-5}) and consequently t_5 is obtained as follows:

$$cT_{3-5} \approx \frac{2L}{R_2} \tag{24}$$

$$t_5 = t_3 + T_{3-5}. \tag{25}$$

Zone VI ($t_6 - t_7$): At t_6, when the current of the input side reaches zero, the voltage on the capacitor equals the input dc voltage as well as the voltage on the switch S_1 (the switch S_2 for T-SSCB).

When both currents of the input side and the output side reach zero, the switch S_3 turns OFF after a safe delay $T_Z = T_{6-7}$.

Zone VII ($t_7 - t_8$): At t_7, S_3 turns OFF and the snubber capacitor starts discharging. As the voltage of the capacitor decays to zero, the voltage of the switch S_3 increases to reach V_{dc}. This is because the resistance value across S_3 at the OFF state (M range) is much higher than the resistance value of R_S (KΩ range). During this interval, the voltage of the capacitor, which has been charged to V_{dc}, discharges to R_S during T_{7-8}

$$T_{7-8} = R_S\, C_S. \tag{26}$$

Zone VIII ($After\ t_8$): At t_8, all components and their voltage and current waveforms return to their normal state before the fault and the interruption is completed, and the converter is ready to restart

$$t_8 = T_{7-8} + t_Z. \tag{27}$$

Table II summarizes the dependency of each time interval to the value of different parameters of the topologies.

III. DESIGN PROCEDURE

The proper values of snubber capacitance and MOV highly affect the performance of SSCB along with time intervals. Therefore, their appropriate design is of high importance.

A. Snubber Capacitor, C_S

Considering $v_C\ (t_4) = V_{\text{clamp}}$ in (11), we have

$$V_{\text{Clamp}} = e^{-\alpha T_{3-4}}\left(\left(\frac{I_P}{C_S}+\alpha V_{\text{dc}}\right)\frac{\sin(\omega_d T_{3-4})}{\omega_d} - V_{\text{dc}}\cos(\omega_d T_{3-4})\right) + V_{\text{dc}}. \tag{28}$$

By considering t→0, the following approximations can be made to simplify the complex equation:

$$e^{-\alpha T_{3-4}} \approx 1,\ \frac{I_p}{C_S} \gg \alpha V_{\text{dc}},$$

$$\sin(\omega_d T_{3-4}) \approx \omega_d T_{3-4}, \cos(\omega_d T_{3-4}) \approx 1.$$

Doing so, the value of the snubber capacitor can be derived from (28)

$$C_S \approx \frac{T_{3-4} I_P}{V_{\text{clamp}}}. \tag{29}$$

By replacing I_P with (6) we obtain the following statement:

$$C_S \approx \frac{T_{3-4}}{V_{\text{clamp}}}\left(\frac{T_{0-2} V_{\text{dc}}}{L_1+L_2} + I_N\right). \tag{30}$$

Since T_{0-2} has a large dependency on the speed of the microcontroller and the current sensor, $L_1 + L_2$ are line parameters, V_{dc} and I_N are constant and predefined, and also V_{clamp} has its own limit, C_S can be optimized mainly by T_{3-4}.

B. Snubber Varistor, MOV

The desired MOV can be selected considering three parameters including V_{clamp}, E_r, and I_{Surge}.

The maximum clamp dc voltage V_{clamp} for T-SSCB and Y-SSCB must be 10% lower than the maximum surge voltage of the switches

$$V_{\text{clamp}} < 1.1 V_{S,\max}. \tag{31}$$

For H-SSCB

$$V_{\text{clamp}} < 2.2 V_{S,\max}. \tag{32}$$

On the other hand, it also must be 10% higher than V_{dc}

$$V_{\text{clamp}} > 1.1 V_{\text{dc}}. \tag{33}$$

The maximum surge current must be less than the current of the input side inductor at t_4. Hence, according to (14)

$$I_{\text{Surge}} < I_P - \frac{V_{\text{MOV}} - V_{\text{dc}}}{L_1} t_4. \tag{34}$$

The surge energy on the MOV during T_{4-6} can be calculated as follows using the derived i_{L1} from (15):

$$E_{\text{surge}} = \int_{t_4}^{t_6} V_{\text{MOV}} i_{L1} dt \approx \int_{t_4}^{t_6}\left(\frac{V_{\text{dc}} - V_{\text{Clamp}}}{\text{t}} + V_{\text{Clamp}}\right)\left(I_P - \frac{V_{\text{Clamp}} - V_{\text{dc}}}{L_1} t\right). \tag{35}$$

TABLE III
COMPARISON OF THE PROPOSED SSCBS WITH THE CONVENTIONAL BIDIRECTIONAL SSCBS

SSCB	Num of switches	Num of diodes	Num of caps	Num of MOVs	Num of inductors	Decoupling of input and output side	Not using switches of the main path	Discharged snubber capacitor before reclosing	Suppressed MOV's leakage current	Common ground
[31], [3]	2	2	2	2	0	No	No	No	No	Yes
[32]	4	0	4	5	0	No	No	No	No	Yes
[33]	2	4	4	0	4	No	No	No	-	NO
[34]	4	0	2	1	0	No	No	No	No	Yes
[35]	6	2	2	0	1	No	No	No	-	Yes
[36]	3	5	1	0	3	No	No	No	-	Yes
[37]	6	2	2	0	1	No	No	No	No	Yes
[27]	6	0	2	2	1	No	No	No	No	Yes
[28]	6	3	2	2	0	No	Yes	Yes	Yes	Yes
[30] (MOV-RCS)	4	0	1	1	0	No	Yes	Yes	Yes	Yes
[30] (AMOV-RCS)	4	4	2	1	0	No	No	No	Yes	Yes
T-SSCB	3	2	2	1	0	Yes	NO	Yes	Yes	Yes
Y-SSCB	3	4	2	1	0	Yes	Yes	Yes	Yes	Yes
H-SSCB	3	4	4	2	0	Yes	Yes	Yes	Yes	Yes

The obtained result is the minimum value of surge energy of the MOV

$$E_{\text{MOV}} > E_{\text{surge}}. \tag{36}$$

IV. COMPARISON RESULTS

The proposed SSCBs have some advantages over the conventional ones, which are demonstrated in Table III. These bidirectional SSCBs are compared by their number of components and five crucial features.

In [31], a bidirectional SSCB is introduced using two back-to-back switches. The voltage on the switches in this SSCB is twice the voltage on Y-SSCB. In addition, after fault detection, it utilizes the second switch along with the fact that the snubbers will create a loop in the circuit including the input and output during and after the fault interruption till reclosing.

Yan et al. [32] utilized a break-over diode to share the system's dc voltage during the standby state and an SCR to provide the bypass path for the fault current. Its main contribution is to decouple the peak clamping voltage of the MOV from the nominal dc voltage of the system aiming to improve the voltage utilization rate resulting in the reduction of the system's conduction losses. However, it uses a high number of components and still has problems of the previous SSCB.

The three topologies proposed in [33] and similar z-source SSCBs mainly rely on multiple sets of reverse parallel thyristors to realize the bidirectional energy flow and they can automatically break the bidirectional fault current. Despite this, the breaking process of these breakers is uncontrollable because it is heavily influenced by the parameters of the outer circuit, so there are too many thyristors and inductive components. There is also a need for more gate-triggering circuits, increasing the complexity of the entire circuit. As the number of inductive components increases, the circuit becomes larger and more costly, and the inductor in the loop makes the load and power supply have no common ground.

The SSCB proposed in [34] has an active and fully controllable opening process with a reasonable number of components, However, it does not provide the rebreaking capability, which is required in IEC-62271-100 to guarantee safe restarts of dc systems by controllably reclosing and rebreaking breakers. The SSCB in [35], solves the lack of control over rebreaking and reclosing by adding two thyristors and two coupled inductors but still lacks the features of the proposed SSCBs in Table III.

The SSCB proposed in [27] along with breaking faults, acts as a compensator for dc networks using series and shunt compensators. However, it lacks decoupling of input and output terminals along with the MOV's degradation issue.

Another SSCB with a third leg is presented in [28] removes MOV from the power line, however, it suffers from high number of switches along with large capacitors.

Another SSCB with a third leg is presented in [28] removes MOV from the power line, however, it suffers from a large number of switches along with large capacitors.

Two bidirectional SSCBs are proposed in [30] that solve the degradation issue of the MOV by removing it from the main power line. However, the MOV-RCS one uses one extra switch in comparison with this article's SSCBs and does not decouple the terminals of the SSCB. The AMOV-RCS uses thyristors for automatic turn-OFF but has to use one of the main switches during breaking and does not discharge the capacitor before reclosing.

V. EXPERIMENTAL RESULTS

Fig. 6(a) shows the schematic of the test circuit of the prototypes and the laboratory prototype of the designed SSCBs is presented in Fig. 6(b). In this test, the short-circuit is created using a mechanical relay K across the load. Two inductors are placed in the input and output terminal of the SSCB as line

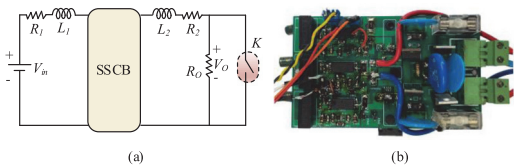

Fig. 6. Laboratory test. (a) Schematic of the test circuit. (b) Laboratory prototype of the proposed SSCBs.

TABLE IV
DESIGN PARAMETERS OF THE PROPOSED SSCBS

Parameter	Acronym	Value
Rated Power	P	Test1: 3.5 kW Test2: 12.5 kW
Input Voltage	V_{in}	Test1: 350 V Test2: 500 V
Nominal current	i_N	Test1: 10 A Test2: 25 A
MOSFETs	S_1, S_2, S_3	UF3SC120016K4S
Diodes	D_1, D_2, D_3, D_4	APT30DQ120KG
Snubber Resistor	R_S	3KΩ
Snubber Capacitor	C_S	500nF, 2kV
Snubber MOV	MOV	Test1: V_{dc} =385 V, V_{Clamp}: 770 V Test2: V_{dc} =505 V, V_{Clamp}: 1000 V
Input side Inductor	L_{Line}	10 µH
Output side Inductor	L_{out}	20 µH
Load Resistor	R_{Load}	50 Ω
Input side Resistor	R_1	1.5 Ω
Output side Resistor	R_2	1.5 Ω

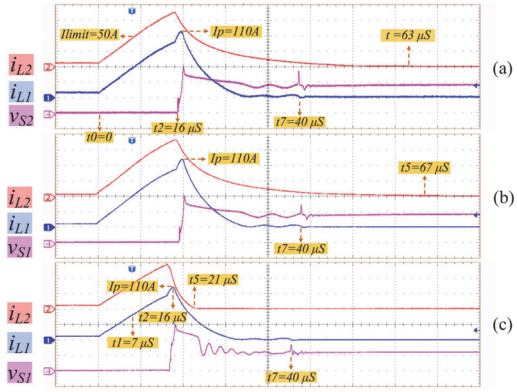

Fig. 7. Test 1 results. The electrical waveforms of the proposed SSCBs. (a) T-SSCB. (b) Y-SSCB. (c) H-SSCB.

inductors with values 10 μH and 20 μH, respectively. The input dc voltage is 350 V in the first test and 500 in the second test and the output resistor is 50 Ω as the load. The complete list of the design parameters is presented in Table IV.

In the first test (see Fig. 7), the nominal value of the circuit's current is 10 A and the limit current of the SSCB is 50 A. The overcurrent is detected and reacts in 9 μS. After the detection and reaction, the current reaches 110 A. Following this, the switch S_3 turns ON, which makes a short circuit across the input side and bypasses the short circuit current into the third leg. To protect the switches, the switch S_2 is turned OFF after a short time interval T_S, which is considered 1 μS here. During this 1 μS, the short current passes through a closer path to the source and sees a lower resistance, therefore, the current increases with a sharper pace until it reaches its peak when the input current starts to plummet. In T-SSCB, the maximum voltage peak voltage of the snubber capacitor and therefore the switch S_2 equals the maximum clamping voltage of MOV, which is 770 V. It takes 47 μS for i_{L2} and 24 μS for i_{L1} to reach zero [see Fig. 7(a)]. When the input current i_{L1} reaches the MOV's leakage value, after a safe interval of 5 μS the switch S_3 turns OFF to completely make it zero.

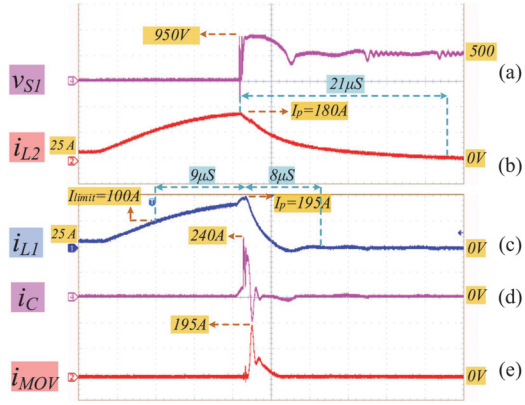

Fig. 8. Test 2 results. The electrical waveforms of the proposed SSCBs for Y-SSCB.

In Y-SSCB [see Fig. 7(b)], the input current passes through the diode D_3. Also, unlike T-SSCB, the source pins of the switches are connected instead of the drains that places the voltage stress on the switch S_1. The results in this case are similar to T-SSCB; However, the current does not pass through any of the power line switches.

H-SSCB has an extra snubber in series with its output side diode making it benefit from faster fault clearance in the load side which is about 5 μS in this test [see Fig. 7(c)]. However, since there is a reverse voltage on the output side snubber capacitor, the voltage of the drain pin of MOSFET S_2 is $-V_{\text{Clamp}}$. Therefore, the voltage across the switch S_1 will be $2V_{\text{Clamp}}$. This structure is suitable in applications where fast fault clearance is needed on both sides and where cost is not a priority and switches with higher voltage can be used.

In the second test (see Fig. 8), the input voltage is 500 V and the nominal current is 25 A. In this case, using a 505 V MOV with clamping voltage of 1000 V, the overvoltage on the switches is 950, as shown in Fig. 8(a). Fig. 8(b) shows the output side current, which reach its peak at 180 A and decays to zero in 21 μS. The voltage experiences an oscillation when the third switch turns OFF. This oscillation depends on the safe delay T_S. As shown in Fig. 8(c) and (e), the peak short circuit current in this test in the input side is 195 A while the limit current to be detected is set to 100 A. The values of time intervals are similar to the first test and are presented in the figure. Fig. 8(d) and (e) shows the current of the capacitor rising at the time of breaking operation and commutating to MOV when the voltage of the switch S2 reaches near the clamping voltage.

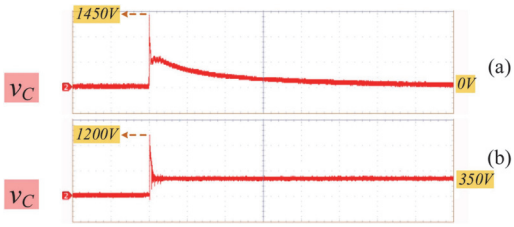

Fig. 9. Voltage of snubber capacitor in. (a) Proposed SSCBs. (b) Conventional SSCB (the SSCB in Fig. 1).

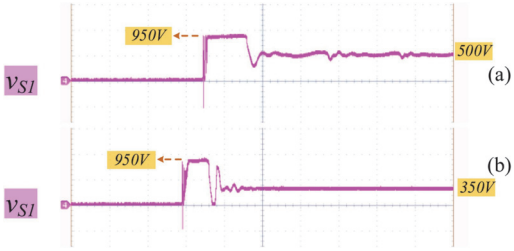

Fig. 10. Overshoot voltage on the switches. (a) Proposed SSCBs. (b) Conventional SSCB (the SSCB in Fig. 1).

The 9 μS reaction time depends on the speed of the microcontroller's program along with the delay of the current sensor. The current implemented current sensor is ACS720KLATR-15AB-T, which has an 8 μS delay. By using a high bandwidth current sensor, the detection time can be decreased considerably.

Fig. 9 compares the voltage of the snubber capacitor in the steady state in the proposed SSCB and a typical conventional SSCB [see Fig. 1(a)]. Unlike the traditional approach, the capacitor in the proposed SSCB is discharged before reclosing. According to (26), the discharging time depends on the value of the snubber resistor.

By analyzing the voltage of the switches in the proposed SSCB and the conventional one in Fig. 10, it is seen that using the same MOV, using a higher dc input voltage is possible in the proposed SSCBs and in general in the SSCBs in which MOV is removed from the power line. In traditional SSCBs with MOV in their power line, the input voltage must be at least 20% higher than MOV's voltage to avoid leakage currents [30].

It is illustrated from the experimental results that the proposed SSCBs can work properly in different voltage levels below the clamping voltage of the MOV with a safe margin, which is attractive for industrial applications.

VI. Discussion

All three proposed SSCBs have the modularity capability to easily extend the current and voltage ratings of the breaker according to the dc system development. However, Y-SSCB and H-SSCB would be better candidates to be modular since in T-SSCB the short circuit current passes through half of the switches, which decreases the reliability.

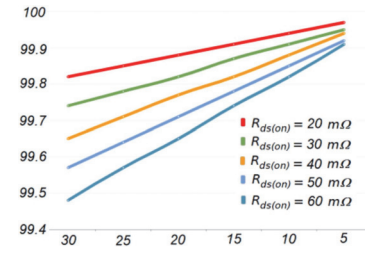

Fig. 11. Efficiency of the proposed SSCBs for different on-state resistances and currents.

A high-efficiency circuit breaker not only demonstrates reduced power losses during consistent operational states but also reduces the necessity for cooling mechanisms. To attain high efficiency in SSCBs, one potential solution is the parallel connection of multiple solid-state switches. This method seeks to lower the equivalent ON-state resistance of the input switch, thus contributing to enhanced overall efficiency. The efficiency of the proposed circuit breakers with the design parameters of the prototype is 99.91 calculated by

$$\mu_{\text{SSCB}} = \left(1 - \frac{R_{ds(\text{on})} \cdot I_{\text{dc}}}{\mu_V \cdot V_{\text{dc}}}\right).100\%. \tag{37}$$

As shown in Fig. 11, the efficiency of the SSCBs decreases as the nominal current or the ON-state resistance of the switches increase. The efficiency figure is drawn by considering $V_{\text{dc}} = 350$. For medium voltage and high voltage applications, the efficiency increases considerably since it is directly proportional to the voltage.

Because solid-state switches are not restricted in terms of their ON/OFF cycles, the lifespan of the breakers is primarily determined by their topology and their operation during the fault isolation procedure. During the isolation process of the proposed SSCBs, no current passes through the switches of the main path, which increases their lifetime and reliability [38].

Due to the low inertia of dc systems and the large rising rate of short circuit fault currents, SSCBs must react to abnormal currents quickly. The response time of an SSCB includes detection and reaction time intervals. The reaction interval is defined from the moment the fault is detected to the time instance in which the line current in the system starts decaying.

The proposed SSCBs benefit from high reliability and increased voltage utilization rate of switches of the main path. In most SSCBs in which MOV is in parallel with the switches, when SSCB is OFF, the voltage of the MOV is equal to Vdc. This leads to reliability problems as a result of the MOV degradation. With an increase in both the number and duration of surge currents, MOVs undergo degradation, leading to a rise in leakage current and a decrease in the time to failure. Moreover, higher temperatures directly influence the leakage current in MOVs, making it proportional to temperature. When an MOV experiences thermal runaway, exceeding its capability, it ultimately leads to a short-circuit failure [39].

To solve MOV degradation in SSCBs, Martin et al. [40] suggested that $V_{\rm dc}$ should be 20 percent less than the maximum allowable dc voltage on MOV in a steady state. Nevertheless, it gives rise to dimensioning challenges and, more importantly, decreases the main thyristor's voltage utilization rate (μ_V) of the switch, which is defined as the following equation:

$$\mu_V = \frac{V_{\rm dc}}{V_{\rm rating,\ Switch}} .100\%. \tag{38}$$

In the proposed SSCBs due to the lack of the MOV in the power line, the maximum allowable dc bus voltage on SSCB and the voltage utilization rate of the switches are increased to at least 20%, which improves efficiency due to (37).

It also increases power density due to extending $V_{\rm dc}$ along with the reduction in the number of series-connected switches for MVdc and HVdc applications and enhancing compactness due to decrease in cooling systems because of using lower switches [30].

VII. Conclusion

A novel family of bidirectional SSCBs was proposed in this article. A complete explanation of all time intervals of the fault interruption was presented along with their calculations to optimize the design. The design procedure section demonstrated that the snubber capacitor's value can be optimized by the time interval from the detection moment to the voltage clamping moment and it a can also be reduced by reducing the detection time. The SSCB takes 9 μS to detect and react to the fault, which is considered fast enough for almost all dc applications. Preparation for the next reclosing takes about 67 μS.

The proposed SSCBs completely disconnect the source and the load side during their operation, and it remains disconnected till the next restart of the system. In the conventional SSCBs, one or several paths connect the input side to the output side during and after the interruption, which lacks human safety along with system safety due to probable oscillation at the output terminal. Removing the snubber from the power line and the main switch; eliminates the MOV's leakage current, which exists in most conventional ones. This also increases the voltage utilization rate of the switches, since during the SSCB OFF-state, the snubber switch holds the dc bus voltage and removes the voltage on MOV. Hence, nor voltage neither power dissipation will appear on the MOV, which leads to increased MOV reliability and voltage utilization rate of the main switches (μ_V). Higher μ_V results in higher reliability due to solving MOV degradation issues, higher power density, design cost reduction, and higher efficiency.

Except for T-SSCB, the proposed SSCBs do not use the switches of the main path during the interruption. Due to the existence of a resistor parallel to the snubber capacitor, the capacitor is completely fast discharged before reclosing.

Among the proposed circuit breakers, T-SSCB is the simplest one, however, Y-SSCB is the optimal option for most dc applications. It uses two more diodes in comparison with T-SSCB, but it does not use any of the switches of the main path, which is a more reliable performance, especially for applications whose reliability is preferred to the cost. In H-SSCB, the time of the fault clearance on the output side will decrease but the voltage overshoot on the switch will increase. So, it is suitable for applications in which the SSCB should start reclosing very fast. Overall, all three bidirectional SSCBs benefit from simple and cost-effective structures compared with conventional bidirectional SSCBs considering the advantages they add.

Despite the useful features of the proposed SSCBs, there are still challenges to address in the future. Fault detection and faster response is one of these challenges. Regarding the proposed SSCBs in this article, the detection and operation time can be reduced in the future using a high-bandwidth current sensors or by proposing enhanced methods of fault detection. Increasing the reliability is another challenge, which means the SSCB can continue to work even when one of its switches burn. Despite the fact that due to rare switching of an SSCB's switches their reliability is already very high, it can still be a challenge in crucial applications such as aircraft and spacecrafts.

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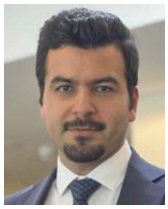

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Dr. Vinnikov is a Chair of the IEEE Estonia Section.

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TOPICAL REVIEW

Fault Management Techniques to Enhance the Reliability of Power Electronic Converters: An Overview

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ABSTRACT The reliability of power electronic converters is a major concern in industrial applications because of using prone-to-failure elements such as high-power semiconductor devices and electronic capacitors. Hence, designing fault-tolerant inverters has been of great interest among researchers in both academia and industry over the last decade. Among the three stages of fault management, compensating the fault is the most important and challenging part. The techniques for fault compensation can be classified into three groups: hardware redundancy methods which use extra switches, legs, or modules to replace the faulty parts directly or indirectly, switching states redundancy methods which are about omitting and replacing the impossible switching states, and unbalance compensation including the techniques to compensate for the unbalances in the system caused by a fault. In this paper, an overview of fault-tolerant inverters is presented. A classification of fault-tolerant inverters is demonstrated and major cases in each of its categories are explained.

INDEX TERMS Reliability, fault compensation, fault-tolerant converter, fault management, multilevel inverter, redundancy.

I. INTRODUCTION

In recent decades, power electronics have been increasingly used in modern power systems. Power electronic converters are the main energy conversion system in a wide range of applications such as renewable energy systems, energy storage systems, smart and microgrid technologies, dc transmission and distribution systems, electric motor drives, and power supplies [1], [2], [3], [4]. The widespread use of power electronic converters in various industries has made their reliable performance a top priority [5].

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Reliability is defined as the ability of an item to perform a required function under stated conditions for a certain period [6]. It is often measured by the probability of failure, frequency of failure, or terms of availability. The essence of reliability engineering is to prevent the creation of failures and faults. A fault in a power electronic system not only may cause an unscheduled interruption, which is not tolerated, but may even lead to a disastrous accident [7], [8]. These unplanned interruptions may cause significant safety concerns and an increase in system operation costs as well [9]. It is therefore clear that the push toward ever-more reliable power electronic products is critical for all industries power networks in rural areas, critical medical equipment power

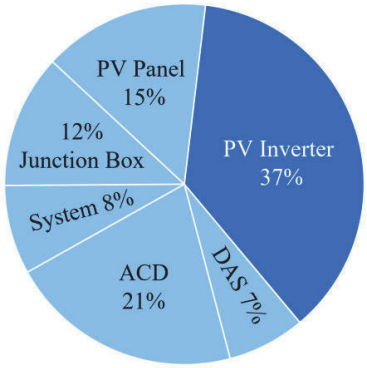

FIGURE 1. Distribution of unscheduled maintenance events of a PV plant.

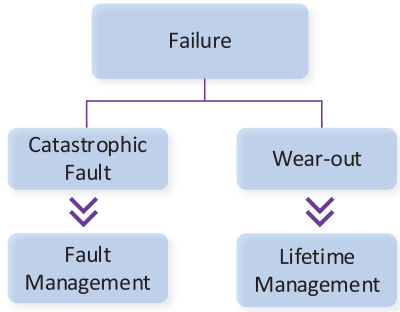

FIGURE 2. Classification of failures in power converters.

supplies, aircraft, and naval power systems, satellite systems with unfeasible maintenance, and wind and solar farm with extensive and widely distributed parts [10]. Considerable manufacturers have been getting a growing awareness of the protection efficiency and maintenance costs of power electronic devices [4]. Hence, the reliability of power electronics is recognized as one of the top research topics, the importance of which is growing rapidly [11].

Inverters play an important role in the reliability of electrical systems such as renewable energy systems, motor drives, electric vehicles, etc. Industrial experiences show drives, electric vehicles, etc. Industrial experiences show that converters are frequent failure sources in many applications such as wind and PV systems [12]. As an example, as shown in Fig. 1, inverters are responsible for about 37 percent of unscheduled maintenance events in PV systems. Therefore, the reliability of inverters is a major concern in industrial applications, especially due to the use of a large number of high-power semiconductor devices with high power densities and high failure rates.

Although there are lots of efforts to make two-level inverters reliable, the fault-tolerant ability is a more significant challenge in the multilevel inverters, as the possibility of failure is higher for these converters due to the higher number of switching devices [13], [14], [15]. Therefore, the study of the fault management operation is mainly focused on multilevel converters.

As shown in Fig. 2, generally, the failure in converters can be classified into catastrophic fault due to single-event overstress and wear-out failure due to the long-time degradation of components. Fig. 3 demonstrates the general guideline for the reliability of power electronic converters. This figure divides the discussion of the reliability of power converters into two aspects: fault management and lifetime management. However, in research, There is usually a distinction between these two reliability areas [16]. Fault management is responsible for managing the catastrophic faults in converters, such as Short-Circuit (SC) and Open-Circuit (OC) faults that can cause destructive damage [17]. The other aspect of reliability is lifetime management, which is mainly concerned with the wear-out issue of the components and devices of the system. It consists of three major subcategories: lifetime analysis, lifetime prediction, and lifetime extension. However, the focus of this survey is just on the fault management aspect of reliability, especially fault compensation and the survey on lifetime management of power electronic converters has been discussed in [16].

Power semiconductors and capacitors are the most vulnerable power electronic components [18]; therefore, the reliability of power converters mostly focuses on these failure-prone power electronic components. capacitors are sensitive to thermal and electrical stresses and have the main disadvantage of low lifespan and high degradation failure rate [19]. It is demonstrated in Fig. 4 that about 18% of the faults in converters are caused by the degradation of capacitors. Electrolytic capacitors, which are mostly used as dc-link capacitors, have the shortest lifetime among all capacitors. These capacitors are among the major failure factors in PV inverters. Many efforts have been done to improve the reliability of power electronic converters by minimizing dc-link capacitance so that small capacitors with a long lifetime can be used to replace electrolytic capacitors. Hence, some research investigations have been devoted to reducing the size of capacitors in inverters as well as replacing the electrolytic capacitors with non-electrolytic capacitors. However, these approaches include extra components along with the increased complexity of the switching patterns. In three-phase applications, a lower amount of capacitance can be used where the power pulsation is lower [20]. In fact, addressing the faults of capacitors is mostly focused on the prevention of faults, and fault management techniques are not discussed in the literature. however, due to the features of the switches, there are many methods that can ameliorate converters' fault conditions.

As was mentioned earlier, generally, the faults in power devices can be divided into two cases: SC fault and OC fault. SC faults affecting the switches are the most serious faults [21]. An SC fault will produce an abnormal overcurrent, causing serious damage to other parts within a very short period of time [22]. Therefore, SC fault-tolerant control

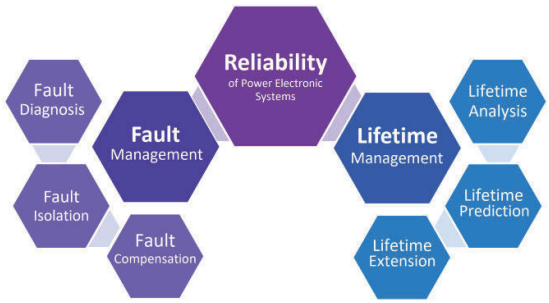

FIGURE 3. Guideline of the reliability of power electronic systems [16].

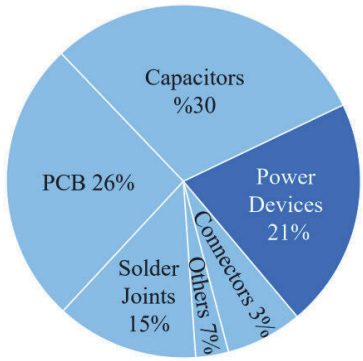

FIGURE 4. Failure distribution among major components in a typical converter.

strategies rely heavily on hardware [23]. This fault is caused primarily by continuous gate pulses, overvoltage, an internal fault caused by overheating, and freewheeling diode failure caused by high reverse recovery voltages [24]. Fast fuse devices connected in series with power devices can convert short circuit faults to open circuit faults whenever the fusible element opens [25].

A variety of mechanisms can cause OC faults, including bond-wire lift-off, gate driver failure, or internal connection rupture caused by thermal or mechanical shocks [26], [27]. The converter operates at low power quality after an OC fault, causing additional stresses on its circuit components, causing secondary problems [28].

When a fault occurs, the fault management operation is activated which consists of fault diagnosis and fault compensation.

This work focuses on methods to compensate for the faults. These techniques of fault compensation in inverters are classified. First, fault isolation techniques are explained which are categorized by hardware-based and modulation-based methods. Then the redundancy methods as the popular approach to reconfiguring the inverter in the post-fault are discussed in detail. Finally, the control techniques to regain the converter's pre-fault performance are described using figures.

II. FAULT DIAGNOSIS

Fault diagnosis or fault detection is the first step once a fault occurs. Fault diagnostic techniques for inverters can be divided into model-based and data-driven methods. The model-based methods are based on the analytical model of the converter [29]. They usually need to consider the dynamic properties and operation mechanism of the system, then establish an accurate mathematical model [30]. The data-driven fault diagnosis methods do not need to know the exact analytical model of the system. they directly analyze and process the measured data [31]. These techniques include signal processing methods, statistical analysis, and artificial intelligence. There is also a hybrid method that uses a combination of these two methods.

It is worth noting that the fault detection method is not the main concern of this paper. In [32], fault Diagnosis techniques for Modular Multilevel Converters (MMCs) are reviewed. References [33] and [34] have evaluated IGBT's different fault diagnosis approaches. References [35] and [36] present a comprehensive survey of fault diagnosis techniques.

III. FAULT ISOLATION

Fault isolation is the first step in tackling a fault in a system. When a fault occurs in an inverter, some switching states may be unavailable due to the SC or OC of the faulty switches. These switching states should be avoided or the faulty components themselves should be isolated so that the system continues to function and prevents damage to the whole system. These schemes are performed by adding some extra elements such as fuses and TRIACs and their goal is to isolate the faulty switch(es). Fault isolation usually results in the degradation of the system's performance, especially in the output voltage and THD. Therefore, there have to be solutions to compensate for the effects of the fault which are discussed in section III.

In Fig. 5(a) [37] one phase of a three-phase two-level inverter is demonstrated. If the switch S_{a2} fails SC, first, the switch S_{a1} should be turned off temporarily. Next, the TRIAC T_a is turned on to make a shoot-through in the bottom dc bus and blow the fuse F_{a2}. Now the S_{a2} is off the circuit. Requiring access to the midpoint of the dc-link and increased parasitic inductance because of the fuses are limitations of this approach.

In Fig. 5(b) [38], [39], when S_{a2} fails OC, S_{a2} and T_a are turned on to create an SC across the top capacitor which blows the fuse F_a. The inverter leg which corresponds to the phase "a" is now isolated. On the other hand, if S_{a2} fails short, turning off S_{a1} is the first step. Then the TRIAC T_a is turned on which causes a shoot through in the bottom dc bus capacitor and blows Fa which isolates the whole leg "a".

In Fig. 5(c) [40], when the switch S_{a2} fails either SC or OC, S_{a1} is turned off and T_{a1} is turned on. This creates a shoot-through that blows the fuse F_{a2} which removes the switch S_{a2} from the circuit. Require a high number of components and increased parasitic inductance because of the fuses. are the

drawbacks of this technique. Also, relatively large capacitors are needed to decrease the isolation time.

In another approach which is shown in Fig. 5(d), after isolating the faulty leg, the neutral point of the three-phase motor is forced to connect to the dc-link midpoint by turning on the TRIAC T_a.

One leg of a three-phase Neutral Point Clamped (NPC) inverter with an isolation circuit is shown in Fig. 5(e) [41], [42]. If S_{a1} fails short, then the top dc-bus capacitor will experience an SC through D_{a2} and F_{a2} during the zero switching state in which S_{a2} and S_{a3} are turned on. To avoid this switching state, T_{a2} is turned on to blow the fuse F_{a2}. The inverter is turned into a two-level inverter where the output voltage is the same as before, but its THD decreases.

In the modified NPC inverter in [43], [44], and [45] (Fig. 5(f)) the faulty phase is forced to connect to the dc-link midpoint via an additional TRIAC. After faults, the reconfigured system is similar to the structure where only four switches are used to drive a three-phase machine. Since the inverter is still capable of providing the full rated current, the maximum balanced line-to-line output voltage in postfault operations is reduced to half of its nominal value. The limitations of this approach are requiring access to the midpoint of the dc-link, and oversized dc-bus capacitors.

ANPC converter shown in Fig. 5(g) can be operated as a three-level leg after a single-switch SC fault [41], [42]. For example, if S_{a1} fails short, thyristor T_{a2} is turned on to blow fuse F_2. However, unlike NPC, the zero state still can be obtained by turning on switches S_{a2} and S_{a5}. The other switching states remain unchanged. After the fault, the output voltage will experience no change in value, however, the voltage stress on the healthy devices equals dc-bus voltage.

The cascaded H-bridge (CHB) inverter shown in Fig. 6, is one of the popular converter topologies used in high-power medium-voltage motor drives to achieve medium-voltage with low harmonic distortion [46]. The wide adoption of Cascaded Multilevel Converters (CMC) and Modular Multilevel Converter (MMC) in the high-voltage direct current (HVDC) industry is mainly due to their modularity, scalability, and inherent fault tolerance [47], [48], [49]. It is composed of a number of modular H-bridge power cells and isolated dc voltage power sources, which can be obtained from the phase-shifting transformer and diode rectifiers [50].

The CMC topology (Fig. 7) has inherent module-level redundancy [47], [51]. If a module e.g., A_1, experiences failure, it is bypassed by the TRIAC T_{A1} and the corresponding healthy modules of two other phases which are B_1 and C_1 can be bypassed for making the voltage balanced [50]. However, as demonstrated in Fig. 7, the symmetry output voltages are achieved with a 33% amplitude reduction, which limits the operation range under fault.

In [52], the suggested structure (Fig. 8) has four relays in each module. The relays mentioned above are connected so that in the event of an SC or OC failure, the defective module can be eliminated and isolated from the whole system, ensuring the normal operation of the inverter with two healthy modules. If a second fault occurs in two remaining modules, the faulty module will be eliminated using the related relays and the output voltage level will be decreased from 7 to 3 so that the remaining modules can continue to operate. The main drawbacks of the mentioned fault-tolerant scheme are the high voltage stress on the remained healthy switches and decreased output voltage level. Therefore, the switching algorithm is modified to allow the inverter to either continue working in nominal condition, if it is possible or in derated operational mode [53].

IV. FAULT COMPENSATION

After fault isolation, fault compensation schemes are required to guarantee the operation of the faulty inverter as close as possible to normal operation. In this paper, as shown in Fig. 9, fault compensation techniques are classified into three groups: hardware redundancy, switching states redundancy, and unbalance compensation control. In order to choose a suitable fault-tolerant method, output performance consisting of factors including the total harmonic distortion (THD) of output voltages or currents, system efficiency, and dynamic response should be considered. Cost is another important factor in comparing different techniques of fault compensation.

Redundancy means that when a feature of a system is down, it can be replaced by another feature that is already included in the system [54]. In the case of inverters, redundancy can be either switching state redundancy, which includes alternative current paths to obtain the same voltage level, or hardware redundancy, which includes extra switches, legs, and modules.

A. HARDWARE REDUNDANCY

Redundant hardware techniques involve adding some redundant hardware to the original system. The addition of hardware increases the cost of the system, but it provides advantages in post-fault operations, especially in applications where cost is not a major concern [8].

A simple solution for switch redundancy is shown in Fig. 10(a) which handles SC of the switches S1 and S2 [55], but it suffers from voltage sharing problems and doubled conduction losses in healthy conditions.

The topology in Fig. 10(b) can resolve both OC and SC faults by using TRIACs [56]. It does not have the problems of the previous topology; however, its cost is higher due to the number of components.

A fault-tolerant switch-redundant flying capacitor leg is introduced in [57]. which is demonstrated in Fig. 10(c). When one of the switches fails, its complementary switch is turned on. The redundant cell is composed of R_1, R_2, C_R replaces the faulty one. The FC leg continues to provide the same output voltage. During normal mode, the additional cell is in a permanent on-state [57].

In the switch-redundant topology in Fig. 11, if one of the upper switches fails OC or SC, it can be replaced by the

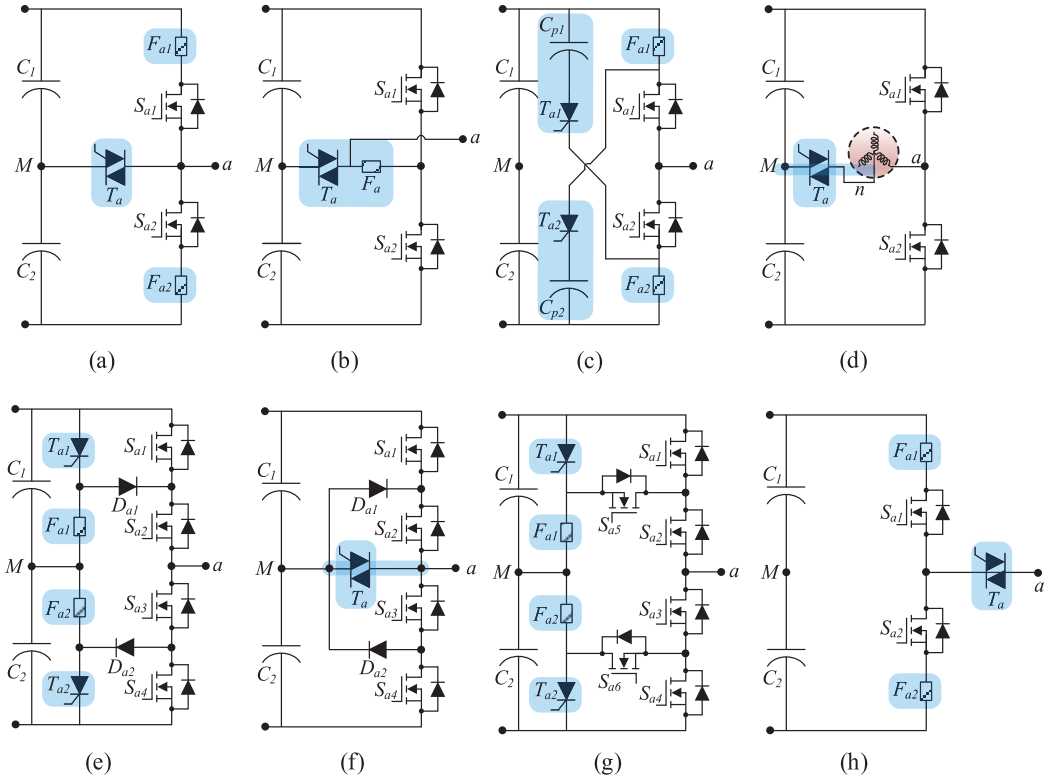

FIGURE 5. Structure of fault isolation approaches.

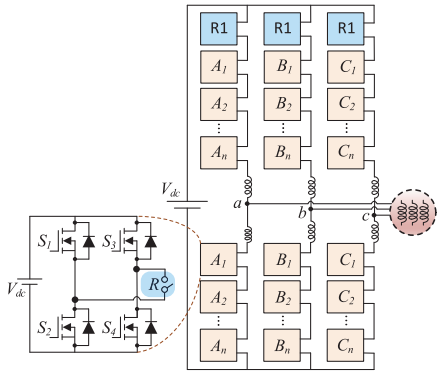

FIGURE 6. Fault-tolerant structure of CHB inverter.

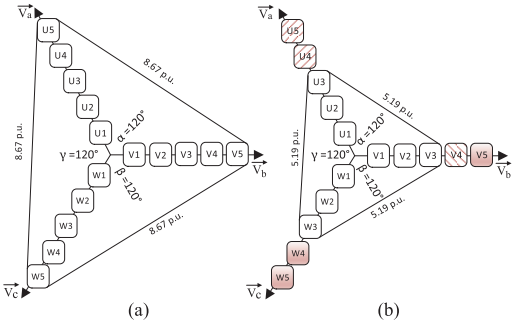

FIGURE 7. The phasor diagram of CMC inverter: (a) normal mode, (b) under fault condition.

redundant switch S_{R1} by the correspondent relay. The strategy for the failure of bottom switches is the same.

The topology presented in [59] proposes a fault-tolerant five-level inverter for PV applications consisting of a two-level half-bridge inverter, a three-level diode-clamped inverter, and a bidirectional switch made with four diodes. As a result of a switch fault or dc-source fault, the topology operates as a three-level, resulting in half the output voltage. Two additional switches and a center-tapped transformer are suggested by [59] in order to maintain the output voltage of the inverter at the same value before the occurrence of the fault.

Some hardware redundant topologies use the redundancy of a whole leg to make the leg replicable when a probable fault occurs. The redundant leg can be connected in parallel or in series.

The converter in [60] is based on a back-to-back converter and S_7 and S_8 as its redundant switches. One leg of this

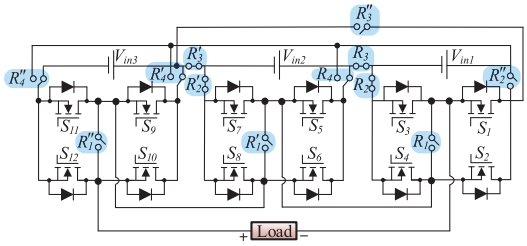

FIGURE 8. The fault-tolerant inverter proposed in [52].

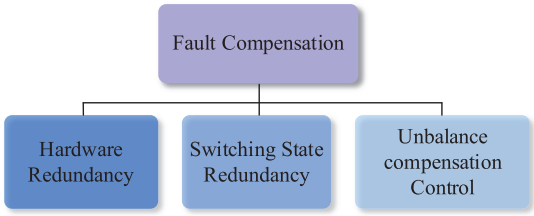

FIGURE 9. Classification of fault compensation techniques for power converters.

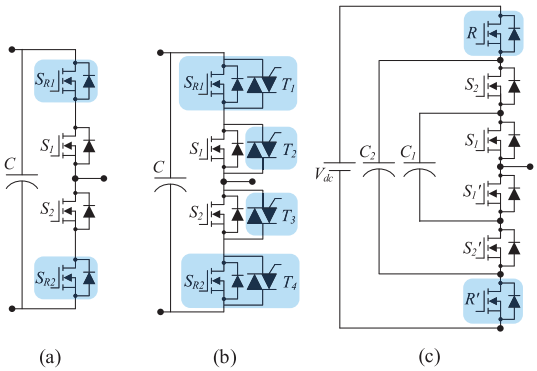

FIGURE 10. Fault tolerant topologies using series switch redundancy.

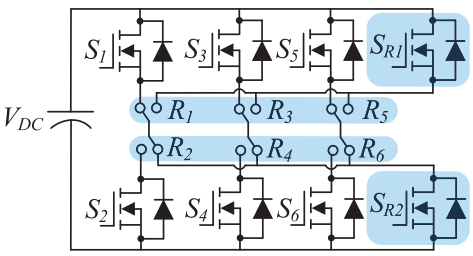

FIGURE 11. Fault-tolerant inverter using parallel switch redundancy proposed in [58].

topology is shown in Fig. 12(a). If one of the switches e.g., S_1 fails OC, the TRIAC T_1 is turned on to connect which makes the faulty leg get replaced with the redundant leg containing S_7 and S_8. In the SC case, the faulty leg is isolated by very fast-acting fuses; consequently, the SC fault becomes an OC fault after the isolation of the faulty leg by the two fuses.

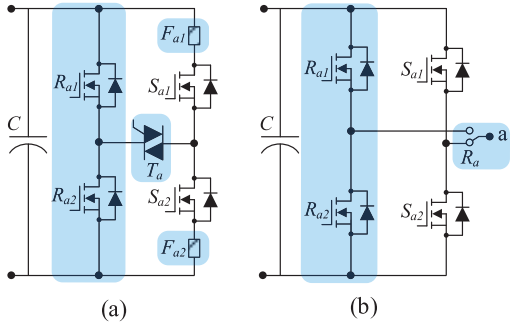

FIGURE 12. Fault tolerant topologies using leg redundancy.

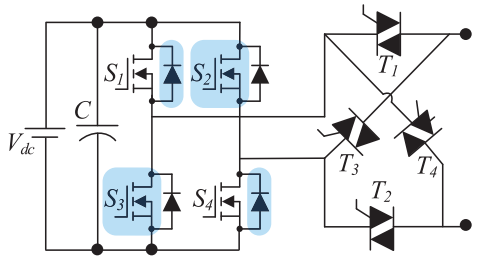

FIGURE 13. Fault-tolerant inverter proposed in [61].

The topology in Fig. 12(b), does not use fuses and TRIAC. Turning on the relay removes the faulty leg and connects the redundant leg. However, it cannot handle two SC switches in one leg.

In [32], as shown in Fig. 13, switches S_2 and S_2 act as redundant switches. In normal operation, during the positive half cycle of the current i_O, the TRIACs T_1 and S_2 are continuously on. The powering ode is obtained by turning on S_1 and S_4 and the freewheeling mode is obtained when either S_1 and D_2 or D_3 and S_4 conduct. During the negative half-cycle of i_O, the TRIACs S_7 and S_8 are on instead of S_5 and S_6. In this configuration, the switches S_1 and S_4 and the diodes D_2 and D_3 are utilized in the same way as in the positive half cycle.

When S_1 fails short, S_4 is turned on to obtain powering mode, and S_4 is turned off to obtain freewheeling mode. In the event of an OC fault in S_1 or S_4, the converter continues to function using S_2 and S_3. In this case, while during the negative half cycle the TRIACs S_5 and S_6 are on, S_7 and S_8 are on during the positive half cycle. During the normal operation, S_2 and S_3 use the same switching strategy as S_1 and S_4. When S_7 experiences an OC fault, S_8 is turned off permanently, and S_5 and S_6 are permanently turned on. As a result, the converter is permanently reconfigured to the conventional VSI configuration. As soon as an SC fault occurs in S_7, S_8 will be turned ON, and S_5 and S_6 will be permanently turned off. and the circuit is permanently changed to the conventional VSI configuration.

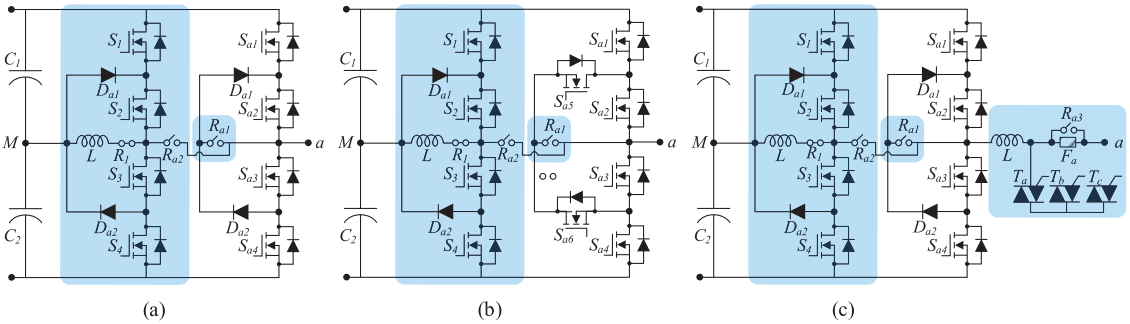

FIGURE 14. Fault-tolerant leg-redundant inverters proposed in [62].

In [62] a fourth leg is added to the conventional NPC inverter which is connected to the neutral point of the converter through an inductance. This fourth leg apart from its duty as a redundant leg for the postfault operation works under the normal operation as well to balance the Neutral point voltage by injecting the locally averaged current to the neutral point. Relays are added to reconfigure the converter as soon as a fault is detected in any of the switches. Due to their inductance being in series, the parasitic inductance of these relays is negligible. From an operational perspective, the first solution in Fig. 14(a) is the simplest. Convertor reconfiguration does not require changing modulation indexes or blowing fuses. Nevertheless, semiconductors must be able to withstand the total dc voltage. As a result, the converter is considerably more expensive, and its use is severely limited. The second solution in Fig. 14(b) can be useful in some applications such as controlling an induction motor. It does not require switches that can withstand the total dc voltage, and its price is the lowest. The third solution in Fig. 14(c) like the previous one does not require switches that can withstand the total dc voltage, and it is not necessary to reduce the modulation index during the reconfiguration process. This solution can be a good option for grid-connected applications.

In the topology in [63], a redundant leg is added to a single-phase five-level NPC (Fig. 15(a)). If the switches S_{a2} and S_{b2} fail OC, in an NPC without the redundant leg, the connections to points P and O are not available for the NPC legs. Hence, the redundant leg R compensates for this fault by using S_{R1} with S_{R2} or S_{R4} to connect the input point P to legs A and B respectively. It also turns on the switches S_{R6} with S_{R2} or S_{R4} to connect point O to legs A and B, respectively. Therefore, the five-level output voltage can be preserved. If the switches S_{A1} and S_{B1} fail SC, the NPC legs cannot provide connections to points P and O, and the fuses F_1 and F_4 must be blown. The switches combinations of (S_{R1} and S_{R2}) and (S_{R1} and S_{R4}) are used to connect the leg A and B, to the point P respectively. Also, the switch combinations of (S_{R2} and S_{R6}) and (S_{R4} and S_{R6}) can connect the neutral point O to the legs A and B, respectively. Some merits of this inverter are tolerating all types and locations of faults with full output ratings, reducing components count, preserving high efficiency in postfault operation, and avoiding the usage of bidirectional switches.

In the topology in Fig. 15(b) proposed in [55], the main inverter comprises a conventional three-level NPC leg and a conventional three-level FC leg along with a redundant bridge at the output terminal as the redundant leg.

When OC failure occurs on the switch S_3, the inverter loses its fourth voltage level. In the negative half of the fundamental cycle, this reduces the load current, which reduces the current through the FC. Which leads to the loss of inherent capacitor voltage balancing. Switching R_2 from the redundant bridge generates the fourth level. And preserves the output power of the inverter. When OC occurs, switches S_3, S_5, S_8, R_2, R_3, and R_4 are activated with appropriate pulses, resulting in the generation of a three-level output voltage waveform. [64] classifies the SC fault of switches in terms of the part of the inverter they make SC, including SC of the input voltage source and SC of the capacitor. In the first case, because of OC across the input voltage source, a fuse will be blown to turn the SC fault into an OC fault which is already discussed. In the second case which is the SC of the capacitor, the inverter operates at equal power levels as before the fault while generating a three-level voltage waveform on the output.

The nine-level leg-redundant topology proposed in [65], consists of two three-level flying capacitor legs that are connected by two controlled switches (Fig. 15(c)). bidirectional switches. It can tolerate OC and SC faults in single and multiple switches and maintains the output power and voltage levels in post-fault operation. The switching scheme in this topology maintains the voltage of the capacitor balanced under pre- and post-fault operations.

There are also module-level redundancy approaches. For CMCs and MMCs, redundant modules are added in series with the basic topology as shown in Fig. 16. Normally, the redundant modules are inactive. Whenever a module experiences a fault, it is isolated, and the redundant module replaces the faulty module to restore normal operation [66].

Reference [67] investigates the effectiveness of using redundant cells by the means of reliability assessment and

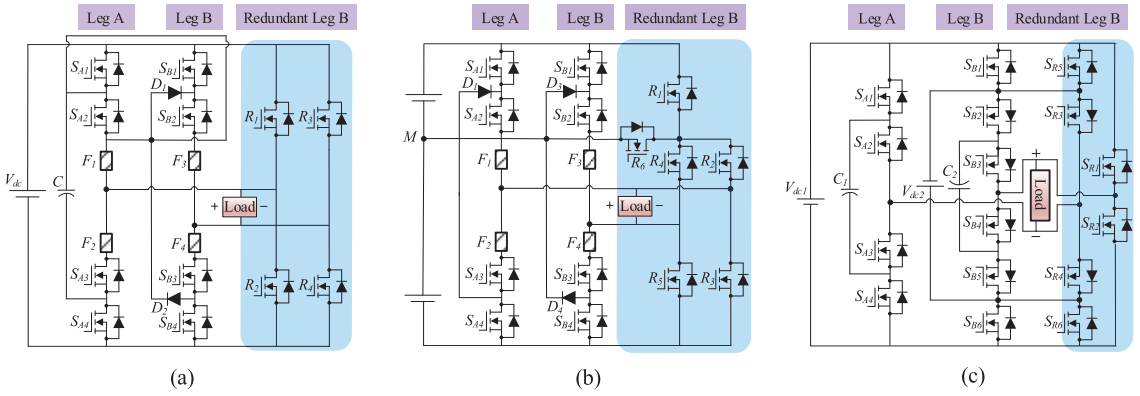

FIGURE 15. Fault-tolerant leg-redundant inverters proposed in (a) [64], (b) [63], (c) [65].

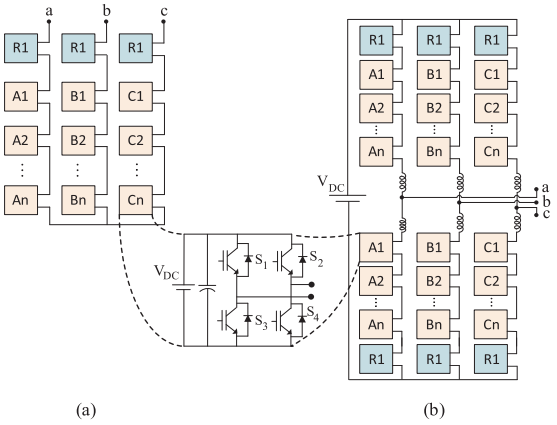

FIGURE 16. Fault-tolerant CMC and MMC with module-level redundancy.

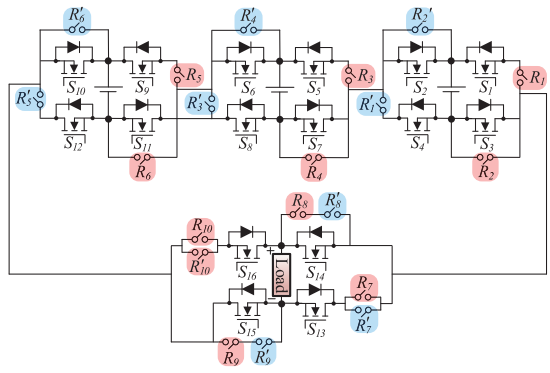

FIGURE 17. Fault-tolerant CHB proposed in [69].

analyses the cost-effectiveness of designs and redundant strategies of MMC.

Reference [68] categorizes the redundancy strategies used in modular multilevel converters into 4 approaches: Standard Redundancy operation (SR), Redundant operation based on Additional Submodules (RAS), Redundant operation based on Additional Submodules Optimized (RASO), and Redundant operation based on Spare Submodules (RSS).

In [69], a fault-tolerant CHB is proposed which uses an extra H-bridge module as shown in Fig. 17. The redundant module just operates after a fault happens. If one of the top switches, in any of the H-bridge cells e.g., switch S1 fails, the top-side relay with the red color in the figure will start functioning. Whenever this relay is triggered, the normal-open conductors of the inverter will be closed, and the conductors that are normally closed will be opened, removing the faulted component from the inverter and the redundant module joins the circuit. when a fault occurs in the bottom switches, the bottom relays in the blue color act and the rest of the action is the same as in the previous case.

If a switch from the top side and one from the bottom side fail together, all the existing dc sources connect to form a set of series-connected dc sources in parallel with the redundant module. However, if a second fault happens, all dc sources connect in series which results in a simple three-level Cascaded Half Bridge (CHB). When one fault occurs, the shape of the output voltage remains unchanged. But, when the second fault occurs the number of the output voltage level reduces to three.

The fault-tolerant inverters using the system-level redundancy are cascaded inverters and parallel inverters. In the cascaded structure in Fig. 18(a), two inverters are connected in series. Although in this approach, several faults including single-switch SC, single-switch OC, and phase-leg OC can be handled, the power rating is reduced after the fault [70].

In the parallel structure in Fig. 18(b), If one inverter fails, the other inverter can replace it so that the system can operate continuously. However, the reduction of circulating currents between converters is an important problem to deal with when the dual converters are performing simultaneously in the normal mode [71].

In the system-level redundant topology in [72] which is shown in Fig. 19, all components including diodes and

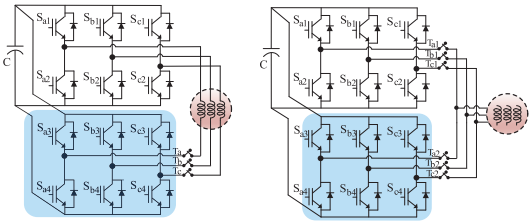

FIGURE 18. System-level redundant inverters (a) Series redundant, (b) Parallel redundant.

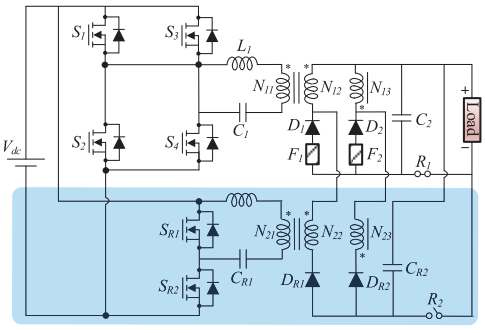

FIGURE 19. Fault-tolerant series-resonant inverter proposed in [72].

capacitors are replaceable by turning on the relay R_1 and turning of the R_2. When one of the switches S_1 to S_4 fails SC or OC, switch S_4 is turned off. Then with the assistance of a second diode D_3 and D_4, the remaining healthy switches S_1 and S_2 are combined with the redundant switches S_5 and S_6 to reconstruct the inverter with the rated output voltage or power. When a diode fails OC, the faulty diode is automatically isolated and when it fails SC, the fuse in series would be melted, thus bypassing it. When C_1 experiences an OC, the faulty capacitor would be also isolated automatically and if SC was experienced, the secondary windings of the transformer T_1 will be shorted melting the fuse F_1. In the case of failure in just capacitors and diodes, since all switches S_1 to S_4 are healthy in this mode, there are four possible modulation strategies. For instance, in a possible switching set, S_3 could be constantly on, S_4 could be always off, and S_1 and S_2 could be complementary.

B. SWITCHING STATES REDUNDANCY

Switching States Redundancy includes avoiding the unavailable switching states and minimizing the impact of the fault by a proper switching sequence. The space Vector Modulation (SVM) approach is typically used to avoid the states involving the failed device. Here, the SVM is represented in an α-β frame which is the conventional technique. The SVM can also be represented in a g-h coordinate system and K-L coordinate system.

In most cases avoiding the unavailable switching states may not be enough to obtain the desired performance of a faulted converter. By adding extra components, using

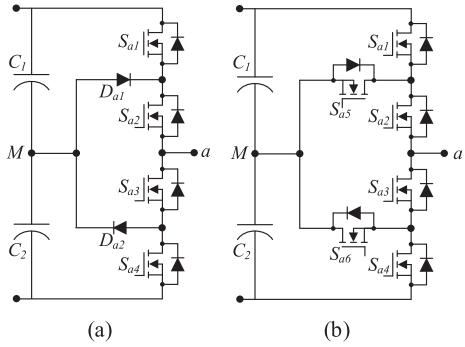

FIGURE 20. One leg of (a) three-phase NPC inverter, (b) three-phase ANPC inverter.

redundant switches, and altering the control strategy, fault-tolerance performance can be achieved which will be discussed in sections III and IV.

In the three-phase NPC inverter of which the leg "a" and its corresponding phase is shown in Fig. 20(a), three types of output switching states are available, positive [P] when S_{a1} and S_{a2} are on, negative [N] when S_{a3} and S_{a4} are on, and zero [O] when S_{a2} and S_{a3} are turned on. If S_{a2} fails SC, the negative state should be avoided because it causes an SC across the bottom dc-bus. In the SVM technique, it is enough to exclude the vectors with N in their phase "a" as demonstrated in Fig. 21. Since these states fall on the output perimeter of the hexagon, the maximum modulation index is reduced [43], [45]. A similar approach can be implemented for SC or OC of the other switches and also the diodes. With this approach, the fault is cleared, however, the modification of the PWM strategy to avoid unavailable states leads to dc-bus mid-point imbalance, spurious fault detection, and overrating of device voltage to full dc-bus voltage [45].

In another approach, the purpose is to change the modulation at the time of the fault in order to make the system survive the impact. Active Neutral Point Clamped (ANPC) converter, which is obtained by replacing diodes in NPC with switches, is widely used in high-power medium-voltage applications including distributed generation such as photovoltaic systems, motor control in traction systems, and industrial motor drives [73]. In this converter as shown in Fig. 20(b) [74], [75], if an OC fault occurs in the switch S_{a2}, the switches S_{a3} and S_{a6} can be turned on to connect the phase voltage to the dc-bus mid-point which minimizes the impact of the fault by reviving the three-phase system.

In this approach, in case of failure, redundancy in the switching states of the inverter, enables the controller to choose an alternate conduction path to retain the same output voltage [76], [77].

In the flying capacitor inverter (FC) as shown in Fig. 22, in the normal mode, the voltage level can be provided by turning on switches S_1, S_3, and S_4 (the current flows through the capacitor C_2 and diode D_2). If for example the switch S_3 fails open, while $i_L > 0$, the same voltage level can be

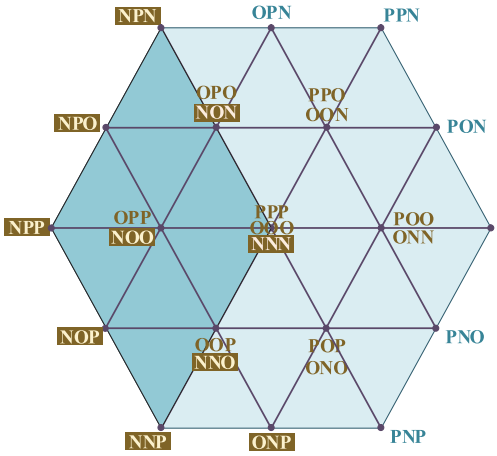

FIGURE 21. SVM hexagon with unavailable switching states as the dashed area.

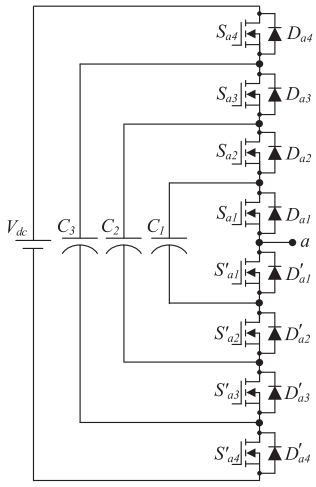

FIGURE 22. Flying capacitor inverter.

obtained by turning on the switches S_4 and S_1 (the current flows through the capacitor C_3 and diodes D_2 and D_3). On the other hand, in the healthy condition, turning on the switch S_2 (the current flows through capacitors C_1 and C_2 and the diodes D_1, D_3, and D_4) the voltage level is produced. If S_3 fails short, while i_L <0, the same output voltage is obtained when current flows through diodes D_1 to D_4. Therefore, the FC inverter benefits from the switching state redundancy which makes it retain its output voltage level after an OC or SC fault occurs.

The four-level MAC converter demonstrated in Fig. 12(a) can always continue operating under a single-device SC and OC fault maintaining at least three of the four levels using redundant switching states. When an SC fault occurs, some

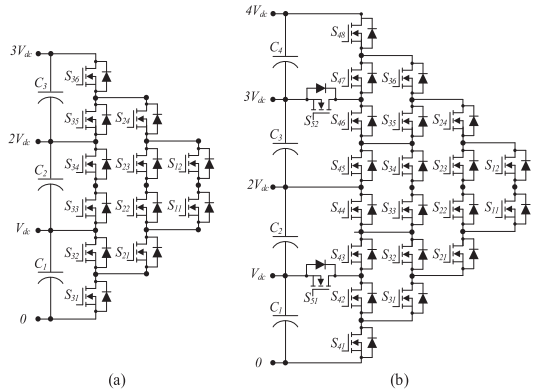

FIGURE 23. MAC topology, (a) traditional one, (b) the proposed structure in [78].

TABLE 1. The possible output voltage levels for two different switching methods of the four-level MAC converter.

priority→	Number of levels					Blocking voltage				
Failed switches	Voltage levels				Over voltage	Voltage levels				Over voltage
	1	2	3	4		1	2	3	4	
S_{31}					No					No
S_{22}					No					No
S_{21}					S_{31}					No
S_{13}					S_{31}, S_{23}					No
S_{12}					No					No
S_{11}					S_{21}					No

switching states will be unavailable. However, they can be replaced by other switching states.

For example, to produce level 1, there is sometimes more than one option to replace the unavailable switching state. Therefore, there are two set modulation strategies in the case of SC. One prioritizes the number of levels and the other one prioritizes the blocking voltage. The produced voltage levels and the switches with overvoltages are demonstrated in Table 1 for both priorities. the possible voltage levels are colored blue. The ones that are achievable by the new switching states are colored with a lighter blue. In the case of two failed switches, the situation is similar to the previous case with the difference that the voltage levels will be either two or three or even four levels.

The topology in Fig. 23(b) is created by adding two additional switches to a MAC inverter [78]. This inverter provides multiple conduction paths in each phase and intra-phase redundancy can be achieved for certain switching states.

In addition, the post-fault control scheme can be Complex. As a result of its redundancy, this topology is limited to a certain output level or semiconductor device. In the case of failure in S_{11}, there is no alternative path and level 1 will be lost. Further, healthy devices may be subjected to increased blocking voltages under certain failure scenarios.

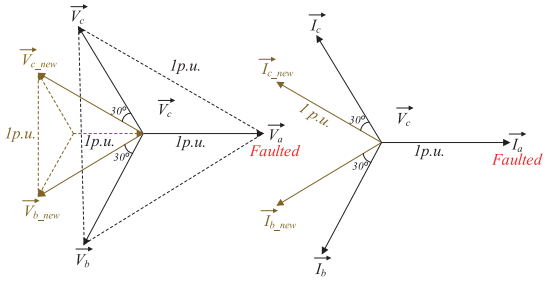

FIGURE 24. Voltage phasor diagram for pre-fault and post-fault.

V. UNBALANCE COMPENSATION CONTROL

Despite the fact that the most important function of an inverter when a fault occurs is to continue servicing as close to normal as possible, other features should also be considered [79]. Imbalance control techniques refer to the altercation of the control strategy to correct the imbalances created by the fault and achieve an optimum operating point concerning the voltage, THD, or any other objective. By using this algorithm, fault-tolerant control can be implemented without changing the inverter's topology. As a result, using them can save hardware costs and simplify topologies [80]. Three techniques of control-based fault compensation methods are discussed in this section.

A. PHASE SHIFT

In the topologies using the dc-link midpoint connection as discussed in section II, when a fault occurs e.g., on a switch in the leg "a", the corresponding phase "a" gets connected to the midpoint of the dc-link through turning on a TRIAC. The reduced system is like a four-switch inverter. To create balanced line-to-line output voltages, the phase angle of the healthy phase voltages (b and c) should be adjusted by shifting by 30 degrees which is demonstrated in Fig. 24 [81].

In the case that the neutral point of the three-phase motor is connected to the dc-bus midpoint, the phase angle of the healthy phase currents (b and c) should be shifted by 30 degrees [82].

B. NEUTRAL SHIFT

When bypassing a module, the voltage and power available from the drive are reduced, but the available current is not affected. As it was mentioned in section II, when a fault occurs in a module in an MMC or CMC, one option after isolation of the faulty module is isolating the corresponding modules in the other two phases to keep the output voltage balanced. However, the output voltage is reduced.

By using the NPS method, there is no need to bypass the corresponding healthy modules and have a balanced output at the same time. As shown in Fig. 25(a), the line-to-line voltages in normal operation are 8.67 p.u.

When modules W_4, W_5, and V_5 experience a fault, the correspondent healthy modules, which are V_4, U_4, and U_5 are bypassed. The new line-to-line voltages are 5.19 p.u.

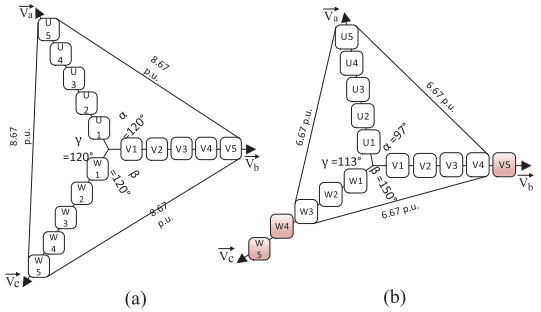

FIGURE 25. The voltage vectors of a modular multilevel inverter (a) Normal condition, (b) Postfault after implementing NPS approach.

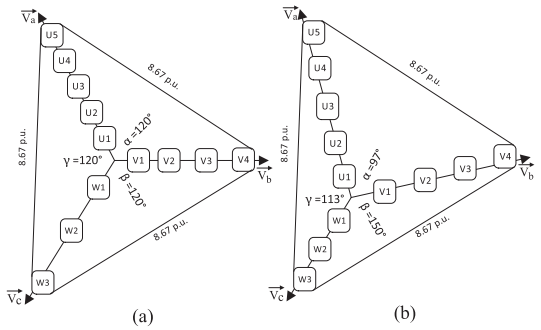

FIGURE 26. The voltage vectors of a modular multilevel inverter (a) Normal condition, (b) Postfault; the overvoltage is shared among three phases.

(Fig. 25(b)). By solving the following equations, we can find the angles between phases that make the voltage balanced [83].

$$V_{ab} = V_a^2 + V_b^2 - 2.V_a.V_b.\cos\alpha \quad (1)$$

$$V_{bc} = V_b^2 + V_c^2 - 2.V_b.V_c.\cos\beta \quad (2)$$

$$V_{ca} = V_c^2 + V_a^2 - 2.V_c.V_a.\cos\gamma \quad (3)$$

$$V_{ab} = V_{bc} = V_{ca} \quad (4)$$

$$\alpha + \beta + \gamma = 360^\circ \quad (5)$$

As shown in Fig. 25(b), the output voltage is higher than the conventional method.

C. EXTENDED NEUTRAL SHIFT

This method is applied in cases in which the converter's neutral point obtained through the traditional neutral-shift approach is located outside the triangle of the output line-to-line voltages [84]. Using this approach, the angle between the two voltages with the lowest amplitude is calculated at 180 degrees, and the amplitude and angle of the other phase are calculated to maximize the output voltage. This method can increase the output voltage by 15%.

D. VOLTAGE EXTENSION

This method is similar to the NPS technique with the difference that the output voltage can be sustained at the same

level as that in the pre-fault condition [85], [86]. An important drawback of the previous reconfiguration strategy is its effect on the common mode voltage, which can lead to unbearable stress on the machine bearings [84]. Many papers including [87], [88], [89], [90], [91], [92], [93], [94] have used this method in their fault-tolerant operation scheme.

To increase the converter's maximum output range, the average of the maximum and minimum reference phase voltages is injected into the common-mode voltages. Fig. 26(a) shows the phasor diagram of the normal operation. When a fault occurs, in order to maintain the output voltage level, the input dc-bus voltage of the faulty phase is increased in order to keep the total voltage unchanged. As shown in Fig. 26(b), the three voltages are balanced, and their value is the same as the normal operation. However, the modules in the phase which had the faulty modules, experience overvoltage. Therefore, to equally share the increased voltage burden among all healthy modules of three phases, optimal angles of the phase voltages are calculated by equations (1) to (5) to obtain Fig. 26(b).

The output harmonic distortion, however, may be significant since this method requires the converter to work in the overmodulation region by injecting excess common-mode voltage [50]. Even though common-mode voltages do not appear in output line-line voltages, they can lead to unbearable voltage stress on motor bearings and shafts. With this method, the fundamental amplitude of the common mode voltage is reduced, resulting in a more bearable operating condition for the load [84].

Not only are there fault conditions without an equation solution or unique solution, but they may also not cause the maximum available voltage.

VI. CONCLUSION

In fault-tolerant topologies, due to the increased number of switches, fault-tolerant converters are more likely to have switch breakdowns than standard converters. However, when these solutions are used, there is a significant decrease in the probability of a complete converter failure, something that is imperative for many industries that use power electronic converters. The first step of fault management is fault diagnosis and after that, fault isolation is considered the primary step to minimize the aftermath of a fault by isolating the fault using extra hardware including fuses, TRIACs, etc. After fault isolation, the effects of the fault must be compensated. The switching state redundancy techniques may use a few extra components to make the possibility of using alternate conduction paths for post-fault, however, these extra component does not necessarily put them in the hardware redundancy category which usually uses the extra switches or legs or modules to replace the faulty ones directly. When a fault happens in the inverter, or even after using a fault hardware redundancy or switching states redundancy methods, there may be imbalances such as voltage unbalance that can be taken care of using enhancing the control strategy of the converter. Choosing the best fault compensation technique first depends on the type of inverter and the application in which the inverter needs to be fault tolerant. Since usually extra components are added in fault tolerance strategies, the cost is an important factor in considering the desired fault compensation solution along with Losses and complexity.

Although various fault-tolerant topologies have been proposed in the last two decades, due to the increase in the demand for reliable systems, there are lots of potentials to propose novel fault compensation ideas, especially imbalance control strategies.

As users may have different main considerations, the suitable redundant designs are application dependent. For a noncritical application, the economy is the main consideration. Although using redundant cells increase the cost of the system, a high level of reliability and survivability of the drive system is essential in some critical industrial processes involving high standstill costs and safety concerns. In addition, lifetime prediction and cost assessment enable us to identify redundant designs that are most cost-effective. Despite the abundance of redundant designs and fault-tolerant algorithms, their reliability improvements remain largely unquantified. Redundancy costs are assessed to determine the cost of fault-tolerant converters in order to provide manufacturers with an affordable option.

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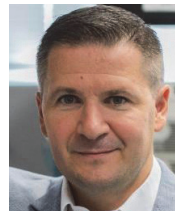

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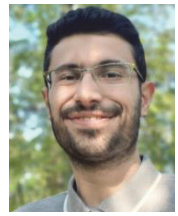

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TOPICAL REVIEW

An Overview of Lifetime Management of Power Electronic Converters

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ABSTRACT An expected lifetime of converters is of great importance for optimal decision-making in the planning of modern Power Electronic (PE) systems. Hence, the lifetime management of power electronic systems has attracted a lot of attention in academia and industry. This paper is a guideline for managing the lifetime of power converters. Analyzing the different kinds of failures, failure modes and their corresponding mechanisms are investigated in the first section along with the failure data needed as input parameters of the assessment. In the second section, lifetime prediction in two aspects of component-level and system level is discussed and all the possible techniques to achieve them are investigated and compared. All the steps required to predict the lifetime in the component-level including electrothermal modeling, cycle counting, lifetime model, damage accumulation, parameter estimation, and lifetime distribution are described and then system level methods consisting of reliability block diagrams, fault-tree analysis, and Markov chains are examined and compared. The last section contains the roadmap of the lifetime extension including the reliable design and condition monitoring.

INDEX TERMS Reliability, lifetime management, lifetime analysis, lifetime prediction, lifetime extension, empirical model, physics of failure, failure mechanism.

I. INTRODUCTION

Using renewable energy systems is one of the most practical solutions for reducing carbon footprint [1]. This technology is powered by power electronics as the core of its energy conversion process. Power electronic converters, on account of their high efficiency and performance, are finding exponentially widespread utilization in various applications such as adjustable speed drives, interfacing of renewable energy sources with the grid, electric vehicles, dc distribution systems, smart grid, and microgrid technologies [2], [3], [4], [5], [6].

The growing use of electronic power converters in various industries has made their reliability a top priority [7]. Power converters' reliability is a major concern in industrial applications because of using prone-to-failure components e.g., high-power semiconductor switches and electronic capacitors [8]. If a component or a subsystem of a power electronic system experiences a fault, it may lead to the shutdown of the whole system [9]. These unscheduled interruptions not only jeopardize safety but also increase the cost of system operation [10]. For example, in hybrid electric vehicles, a fault in electric propulsion systems impairs fuel economy and

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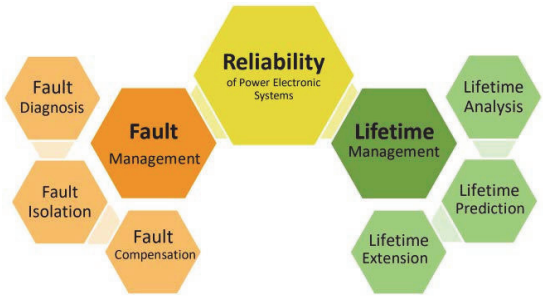

FIGURE 1. Guideline of the reliability of power electronic systems.

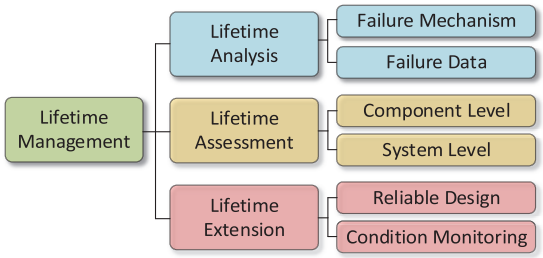

FIGURE 2. Roadmap of lifetime management.

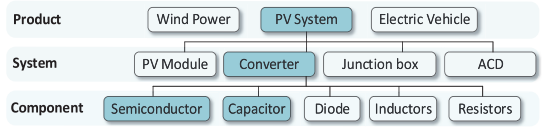

FIGURE 3. Structure tree of a power electronic system, considering PV system as an example.

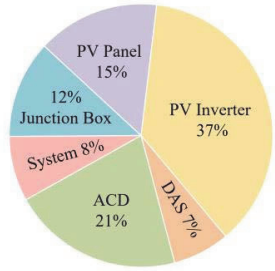

FIGURE 4. Distribution of unscheduled maintenance events of a PV plant [2].

lengthens the cost recovery period. In a photovoltaic system, the cost of failure is equal to the value of the energy that would be generated while the system is down plus the cost of repairing and replacing the faulted parts [11], [12].

Fig. 1. depicts the general guideline for the reliability of the power electronic based systems. As shown in this diagram, power converters' reliability can be discussed from two aspects including fault management and Lifetime management. These two areas are mostly considered as two distinct subjects in research. Fault management deals with sudden catastrophic faults in the converters including short circuit and open circuit. It is about protecting the systems from faults by using circuit breakers and diagnosing and configuring the faults when they have already happened. Lifetime management is the other aspect of reliability which is mostly about predicting and extending the lifetime of the power converters. It consists of three major subcategories: lifetime analysis, lifetime prediction, and lifetime extension as shown in Fig. 2. This survey focuses only on the lifetime management aspect of reliability.

Reliability analysis, which contains identifying the prone-to-failure components along with the mechanism of the failures, is the fundamental step for lifetime management. The short lifetime of power electronic devices is mostly due to thermal stresses in their switching devices such as IGBTs and MOSFETs, especially in high switching frequencies. It can cause the failure of these components which leads to either a catastrophic failure (i.e., open-circuit and short-circuit) or a wear-out failure which causes unreliable performance in the operation of the system. Hence, an appropriate assessment procedure is required to improve the reliability of the converters and particularly their switching devices [13].

Predicting the lifetime of power converters is very important for converter manufacturers and operators [14]. Different from the conventional performance indices for power electronic systems, e.g., power density, efficiency, total harmonics distortion, etc., reliability is a concept that is difficult to measure and quantify. Traditional approaches utilize the data of the reliability handbooks for predicting the probability of random chance failures within the useful lifetime. However, the wear-out failures affect the converters' long-term performance, and therefore predicting and assessing the lifetime of these kinds of failures is done using either model-based lifetime prediction methods or data-driven methods [15].

The structure tree tool can provide a graphical representation of the system structure and identify the interactions between the several subsystems or components of the PV systems. An example structure tree of a typical PV system is given in Fig. 3 in which the PV system can be divided into several independent systems (e.g., PV module, PV converter, junction box, and ACD), which can then be further classified into different subsystems. Among various power products at the system level in Fig. 3, according to the pie chart shown in Fig. 4, the reliability of PV systems is severely affected by inverters. In fact, inverters are very much subject to failures with about 21 percent of the unscheduled maintenance events of a PV plant [2], [16]. From the system-level to the component-level, among the different components of an inverter, capacitors, power switches and PCBs are the most critical elements in case of failure as demonstrated in Fig. 5 [17].

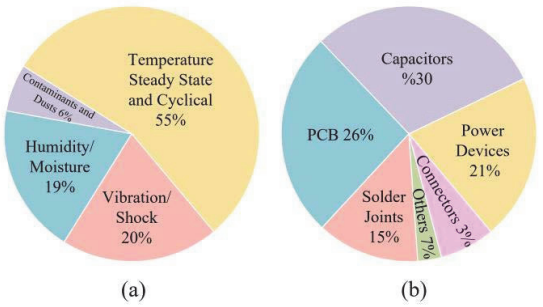

FIGURE 5. Surveys on failures of converters: (a) Distribution of sources of stresses for failures of electronic equipment [2], [16] (b) Failure distribution among major components in a typical converter [2], [19], [20].

In this paper, first, the lifetime analysis including the failure modes and mechanisms of power devices are investigated. Also, various kinds of failure data as the input of the process of assessing reliability are explained. Then, the lifetime prediction methods are examined from two aspects one of which is component-level including handbook-driven, model-driven, and data-driven techniques and the other one is system-level. The third part of the paper deals with increasing the lifetime by using a reliable design process the necessity of which is undeniable for any electronic product. This section also discusses conditioning monitoring which offers benefits for maintenance scheduling and reduced downtime.

II. LIFETIME ANALYSIS

The reliability analysis of a converter is the first step to assessing and expanding its lifetime. It consists of investigating the failure mechanisms of different components of a system along with identifying the failure data of the assessment [18]. The fundamental failure mechanisms of the power electronic components and the way they affect the reliability along with the stressors such as vibration, temperature, cosmic radiation, humidity, and the interactions between them during the operation is necessary to know. An understanding of the input failure variables including environmental stressors, field data, and historical data from the handbooks process of predicting the lifetime is vital to know [21].

A. FAILURE MECHANISM

The purpose of this part of the analysis is to identify the most critical components in a power electronic system, their major failure modes, mechanisms, indicators, and their corresponding stressors causing the failure [22], [23].

Fig. 5. shows the failure rate of critical components of an inverter. As the core part of the drive system, the power semiconductors are very prone to failure due to their frequent on-off switching and the influence of thermal and electrical overstress. Fig 5(a) indicates that temperature is the most dominant stressor of electronic equipment with 55 percent of the distribution. Fig 5(b) represents that power devices such as IGBTs and MOSFETS account for about 21% of an inverter's failures [24]. It also shows that the capacitors have the highest failure rate in power converters. In the absence of redundancy and reconfiguration in a converter, a failure of these components leads to a system's failure, which is considered catastrophic for mission critical converters [18]. PCB is the second highest failure-prone component of a converter with 26 percent chance of failure. Some PCBs' failures happen because of accumulated damage and fatigue and others can be erratic (random), or sudden due to the shocks.

Typically, there are multiple failure mechanisms associated with a specific component each of which should be evaluated individually. There are various failure mechanisms at the chip, packaging, and component levels. Hence, in a complex system where there are a limited number of models and associated parameters, the Physics of Failure (PoF) may be difficult to apply. Thus it is important to identify and focus on the critical failure mechanisms in specific applications [25].

In the following, the failure mechanisms of two major critical power electronic components are discussed and stressors and failure modes of each failure mechanism are explained in tables 1 and 2.

1) POWER SEMICONDUCTOR SWITCHES

Power semiconductor devices are considered as one of the most reliability-critical components in a power electronic system [26]. Failure modes of power switches are either chip-level or package-level [27]. These structures for a SiC MOSFET are shown in Figs. 6 and 7 respectively. Table 1 summarizes important overstress failure modes and their corresponding failure mechanisms [13].

Most chip-level failure modes are associated with gate oxide and body diode. The body diode failure of power MOSFETs is basically caused by stacking faults. Chip-level failure modes of SiC MOSFETs mostly occur at the gate oxide and body diode. Gate oxide degradation failure is primarily caused by the tunneling current into the gate oxide layer [28]. High electric field stress and high-temperature stress also contribute to gate oxide degradation [23]. The gate leakage current i_{gss} would increase. It leads to the increase of both the threshold voltage shift and drain leakage current. The body diode failure is normally caused by the recombination-induced stacking fault mechanism. The main cause of the body diode degradation is the forward voltage bias stress [29] which leads to an increase in forward voltage and drain leakage current.

Bond wires and solder layers are the main locations for the package-level failures of SiC MOSFETs. Fig. 7 shows the typical package-level structure of a SiC MOSFET which is mainly composed of the chip die, the baseplate, and the bond wire. Solder layers connect the baseplate and the substrate and also the substrate and Si chip. Solder film between the ceramic substrate and the baseplate is the most vulnerable to failures [30]. There are mainly three stresses causing the package-level failures as follows [31]. Thermomechanical

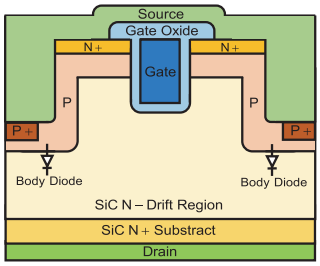

FIGURE 6. SiC MOSFET chip-level structure.

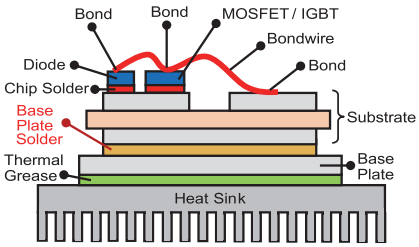

FIGURE 7. SiC MOSFET package-level structure.

stress caused by the CTE mismatch among different materials results in temperature swings leading to solder-fatigue, crack growth, and bond wire failures. However, the highest thermo-mechanical stress that solder joints will be exposed to is occurred during the cooling phase after soldering. [32] The continuous thermomechanical stresses result in the formation of voids and cracks in the solder layers and reduce the effective area accessible for heat loss reduces leading to a rise in the module thermal resistance. This further results in an increase in the device junction temperature which may cause acute localized heating; further possibly leading to catastrophic burnout [33]. Humidity is the second main stress which intensifies the impacts of mechanical stresses, causing a plummet in the metal atom bonding energy. Therefore, the crack growth rate at the tail of the bond wire increases due to atom corrosion. High current density stress is the third stress caused by the relatively small SiC die-size. It leads to acceleration in electromigration-related degradation [34] causing high junction temperature in bond wires which further leads to the increase of on-state drain-source voltage and resistance [35].

Despite identifying several different failure mechanisms, currently, most lifetime prediction models mainly focus on package-related failures.

For IGBTs, failure locations, modes, mechanisms, causes, and indicators are mostly similar to Table 1 with some differences. For IGBTs, failure indicators for gate oxide failure are gate leakage current and Miller Plateau time duration. For solder layer failure, the indicators are voltage change rate, current change rate, junction temperature, and low order harmonic [42], [43].

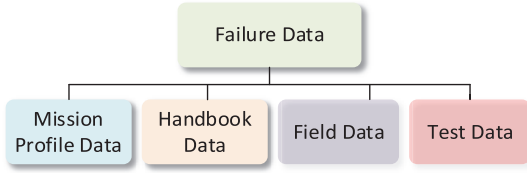

FIGURE 8. Different types of failure data for lifetime prediction process.

2) CAPACITORS

Capacitors play an important role in power electronic circuits as they are used to absorb harmonics, suppress dc-link voltage ripple, provide sufficient energy for transient and abnormal operations, and balance the instantaneous power difference between the front-end and rear-end of converter systems [44], [45]. They are also used as dc-link in applications such as grid-connected inverters, adjustable speed drives, photovoltaic applications, and power factor correction converters. However, capacitors are considered the most reliability-critical components in power electronic converters. Their sensitivity to electrical and thermal stresses results in the disadvantage of a high degradation failure rate [46]. As shown in Fig. 5, about 30% of converter failures are due to the degradation of capacitors [47].

Generally, three types of capacitors used in dc-link applications are electrolytic capacitors, ceramic capacitors, and film capacitors [45] of which failure mechanisms, modes, causes, and indicators are shown in Table. 2.

B. FAILURE DATA

The failure data is the input of the lifetime prediction process. As demonstrated in Fig.8, the failure data can be classified into mission-profile-based data, historical data, and the data derived from accelerated tests as test data [18].

1) MISSION PROFILE

A mission profile is the defined operating conditions of a system which may include internal parameters such as voltage, power, speed, etc., and/or external parameters e.g., temperature, irradiance, humidity, altitude, etc. [47]. In other words, a mission profile quantifies the total amount of stress applied to a system during operation [47]. A mission profile can be defined in different time scales, e.g., a minute mission profile or an annual mission profile. Typical mission profiles for power electronic systems can be the wind speed in wind energy, solar irradiance in photovoltaic applications, speed and torque variations of the electric machine in motor drive applications, output voltage and current operating ranges, customer usage behavior, and also the environmental factors like temperature, humidity, vibration level, etc. [48]. In the case of PV applications, the solar irradiance and ambient temperature are considered as mission profiles [49]. Since producing photovoltaic energy is highly dependent on these two parameters, the mission profile of the PV system can

TABLE 1. Location, modes, mechanisms, causes and indicators of failures in MOSFETs.

Failure location		Failure modes [36]	Failure mechanisms [37]	Failure Causes [38]	Failure Indicator [18, 39]
Chip-Level	Gate oxide	Short-circuit, Increased gate leakage current, Increased gate threshold voltage.	Electrical overstress and ESD, Time-dependent dielectric breakdown.	High electric field, Gate voltage exceeds its breakdown voltage, High temperature	Threshold voltage shift, Drain leakage current, Miller Plateau voltage amplitude.
	Body diode	Increased drain leakage current	recombination-induced stacking.	The forward voltage bias stress	Drain leakage current, Body diode forward voltage.
Package-Level	Bond wires	Increase on-state resistance, Open-circuit.	Bond wire cracking and lift-off, Al Corrosion, bond wire melting.	high temperature, CTE mismatch, Thermo-mechanical stresses	Drain-source on-state voltage, Drain-source on-state resistance, Thermal resistance, Bond wire resistance.
	Solder layers	Open-circuit.	Solder fatigue	high temperature, CTE mismatch, High current density	On-state drain-source voltage, Solder layer resistance.

TABLE 2. Failure location, modes, mechanisms, causes and indicators of capacitors.

Capacitor	Failure modes [36, 39]	Failure mechanism [36, 40, 25]	Failure Causes [30]	Failure Indicator [41]
Electrolytic capacitors	Open-circuit	Self-healing dielectric breakdown	Voltage stress, ambient temperature, ripple current stress,	capacitance, equivalent series resistance (ESR), the dissipation Factor, the insulation resistance, leakage current
		Disconnection of terminals	vibration	
	Short-circuit	Dielectric breakdown of the oxide layer	Voltage stress, ambient temperature, ripple current stress	
	Performance drift	Electrolyte vaporization	ambient temperature, ripple current stress	
		Electrochemical reaction including oxide layer degradation and/or anode foil capacitance drop	Voltage stress	
Film capacitors	Open-circuit	Self-healing dielectric breakdown	Voltage stress, ambient temperature	
		Connection instability by heat contraction of a dielectric film	ambient temperature, ripple current stress	
		Reduction in electrode area due to the oxidation of evaporated metal	Humidity	
	Short-circuit	Dielectric film breakdown	Voltage stress	
		Self-healing caused by overcurrent	ambient temperature, ripple current stress	
		Moisture absorption by film	Humidity	
	Performance drift	Dielectric loss	Voltage stress, ambient temperature, ripple current stress, humidity	
Ceramic capacitors	Open-circuit	Severe cracking	Ambient temperature, ripple current stress, vibration	
		Dielectric breakdown	Voltage stress, ambient temperature, ripple current stress	
	Short-circuit	Cracking; damage to the capacitor body	vibration	
	Performance drift	Oxide vacancy migration; dielectric puncture; insulation degradation; micro-crack within the ceramic	Voltage stress, ambient temperature, ripple current stress, vibration	

vary widely depending on the geographical locations of installation [50]. In electric vehicles, the torque–speed curve over time determines the operating conditions of the power electronic converters within the drive system, which finally affects the electrical and thermal stresses of the key power components.

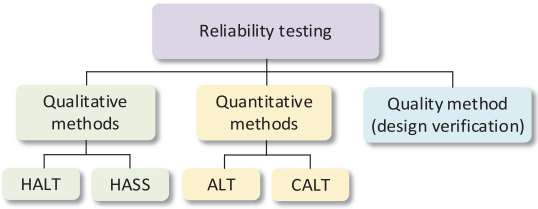

FIGURE 9. Classification of reliability tests.

2) HANDBOOK DATA

In traditional power electronic engineering, the reliability is modeled based on historical data provided by reliability handbooks such as MIL-HDBK-217F. Although the data in most of these handbooks are considered to be outdated and their corresponding prediction approaches suffer from poor accuracy, some of these handbooks like FIDES are still popular in some applications [51]. A summary of commonly used handbooks is provided in Table 3.

3) FIELD DATA

Field Data is a record of the product's performance for its customers provided from call centers, return approvals, exchanges, repairs, and warranty claims, all provide information on field failures. It includes all stresses, expectations, and component variations. The recorded data can be the installation date, the date of failure, usage conditions, failure modes, and failure mechanism.

4) TEST DAT

There are three types of reliability tests as demonstrated in Fig.9. In Accelerated Lifetime Test (ALT), in order to simulate the wear-out failure modes and their corresponding stressors in the laboratory environment, the stresses experienced in the field are applied to accelerate some of the dominant failure modes the component experiences in the field [52]. Calibrated Accelerated Lifetime Test (CALT) is similar to ALT in some aspects but it is applied when the available test time is limited which is described in detail in [53].

Qualitative accelerated lifetime tests including Highly Accelerated Lifetime Tests (HALT) and Highly Accelerated Stress Screening (HASS). These tests are used to find the main weak-points points and are usually employed during more mature stages of the design development, when a functional product-level, system-level, or component-level prototype is already available.

In the HALT approach, the purpose is to make some cases fail under specific test conditions and discover as many failure modes as possible in order to provide failure data for the dominant field failure modes [18].

Qualitative testing approaches tests are applied to determine the robustness of the product design, while quantitative lifetime tests are performed to find the reliability performance of the product [54].

There are also quality (or design verification) testing methods that are employed to ensure that an application-dependent set of specific requirements such as international standards (e.g., IEC 60747, IEC 60384 1401, JESD 22 1411) is met [55]. For instance, power modules are required to undergo a series of tests such as mechanical shock, temperature cycling, power cycling, high-temperature reverse bias, high-humidity reverse bias, and low-temperature storage test to ensure a certain level of quality. Similarly, the capacitors need to pass a series of environmental and expo-sure qualification tests such as thermal shock, high temperature, damp heat, vibration, charge, and discharge to be considered as a market-ready qualified product [38].

III. LIFETIME PREDICTION

The optimal and reliable converter manufacturing, including cost-effective design, decision-making on investment, operational planning, and maintenance scheduling, requires a deep understanding of the system's reliability. Moreover, analyzing novel converter topologies, switching schemes, redundant operation, control schemes, and evaluating the effect of operating conditions on the long-term performance of converters needs a proper lifetime model of the converter. Hence, the lifetime prediction of power converters is of great importance to be carried out [23]. The lifetime estimation of a system is first made by using the component-level models to estimate the failure rate of each component. Then the provided failure rates are summed to generate the system-level lifetime estimation.

A. COMPONENT LEVEL LIFETIME PREDICTION

The failure rate $\lambda(t)$ is one of the widely used reliability metrics in reliability engineering. It is defined as the frequency at which a component or a system fails [56]. Based on the conventional life cycle bathtub curve, as demonstrated in Fig. 10 there are three regions for the failure rate of electronics devices over time including early failures, constant random failures, and wear-out failures [57], [58].

The first part of the curve is dedicated to early failures. A high number of failures occur during this period due to errors in the design phase or the manufacturing process. However, the failure rate decreases over time due to removing the failed and defective products at the beginning of the stage. By performing burn-in or screening tests, early life failures can be addressed.

The constant phase of the diagram, placed in the middle part of the curve, describes the useful lifetime of a product. This stage contains random failures which are typically caused by random fluctuations and transients of stresses exceeding the strength of the component or mishandling of the product [59].

The third part of the curve consists of the wear-out failures of a product. Similar to the human body, as the product including its components and materials ages, the occurrence of failures increases. As an example, the failure of power switching devices at this stage is usually caused by corrosion,

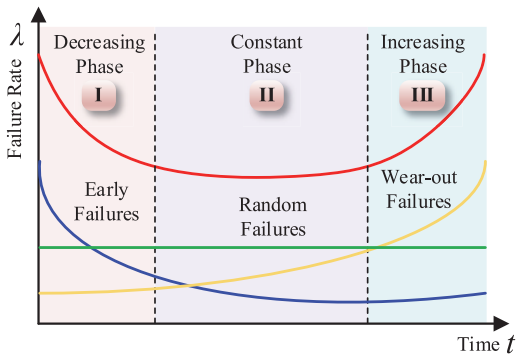

FIGURE 10. Bathtub curve of the failure rate.

oxidation, or fatigue. Increasing the service time makes the wear-out failures dominate the failure probability [60].

A fundamental step for investigating the lifetime prediction of products is understanding the metrics used in reliability engineering [14], [21].

Failure rate as the frequency of failure over time is described as follows: [61].

$$\lambda(t) = \frac{-1}{R(t)} \frac{dR(t)}{t} \tag{1}$$

The reliability $R(t)$ can be represented as the probability of functionality of a product at a certain time [62]:

$$R(t) = \exp\left(-\int_0^t \lambda(\tau)\, d\tau\right) \tag{2}$$

Similarly, the unreliability $F(t)$ can be defined as the percentage of a group of products that fail at a certain time t which can be calculated as follows [3]:

$$F(t) = 1 - R(t) \tag{3}$$

Mean Time to Failure (MTTF) represents the expected time to failure for a non-repairable system. A larger MTTF indicates higher reliability and a lower failure rate [61].

$$MTTF = \int_0^\infty R(t)\, dt \tag{4}$$

Classification of lifetime prediction Methods is shown in Fig. 11. In the first step, lifetime prediction methods are divided in aspect of the type of failures: random failures and wear-out failures. There are also hybrid methods that combine the different techniques of the two major categories.

1) RANDOM FAILURES LIFETIME PREDICTION

Handbook-driven prediction methods are based on models developed from statistical curve fitting of historical failure data, which may have been collected in the field or from manufacturers. These methods tend to present reliability estimation for similar or slightly modified components.

Random failures happen in the constant phase of the bathtub curve of failure rate [63]. Therefore, by considering failure rate is considered constant in (2), the component reliability over time "t" can be expressed as:

$$R(t) = e^{-\lambda t} \tag{5}$$

By replacing (5) in (4), MTTF is equal to the reciprocal of the failure rate:

$$MTTF = \frac{1}{\lambda} \tag{6}$$

Due to ease in dealing with a constant failure rate, the exponential distribution function has proven popular as the traditional basis for reliability modeling. The reliability parameters using exponential distribution are demonstrated in Fig. 12. These parameters are reliability function $R(t)$, Probability Distribution Function (PDF) $f(t)$, which for constant failure rate is λ times more than reliability function, hazard rate $h(t)$ which equals to λ and unreliability function or Cumulative Distribution Function (CDF) $F(t)$ which has been presented in Eq. (3).

The most common handbook used for lifetime estimation is the Military Handbook 217 (MIL-HDBK-217) which was first released in 1991 [64]. This approach suffers from being too general and application independent along with being imprecise as it does not take into consider the root cause of the failures. It is a simple lifetime prediction method that considers only the constant phase of the failure rate curve including random failures and neglects the wear-out stage. Generally, MIL-HDBK-217 failure rate predictions are more pessimistic than other reliability handbook predictions. However, this is variable and depends on the components.

MIL-HDBK-217 standard consists of two approaches for assessing reliability including Parts Count Analysis (PCA) and Parts Stress Analysis (PSA). The PCA technique requires less information such as part quantities, quality level, and application environment. It is most applicable during the early design or proposal phases of a project. This method does not factor in the numerous variables and uses worst-case generic or base failure rates and pi factors. PCA usually results in a more conservative result with a higher failure rate or lower system reliability than PSA. PSA requires more detailed information and is usually employed later in the design phase. PSA approach typically results in a lower failure rate or higher system reliability than PCA. A similarity between PCA and PSA is that both prediction techniques use relatively similar formulas.

PCA utilizes only the estimated values whereas in the PSA method calculated and measured values are used. The general the formula for calculating the failure rate in this method is as follows [65] in which λ_b is the base or generic failure rate and other parameters are introduced in Fig. 13.

$$\lambda_{MOSFET} = \lambda_b \times \pi_T \times \pi_A \times \pi_Q \times \pi_E \tag{7}$$

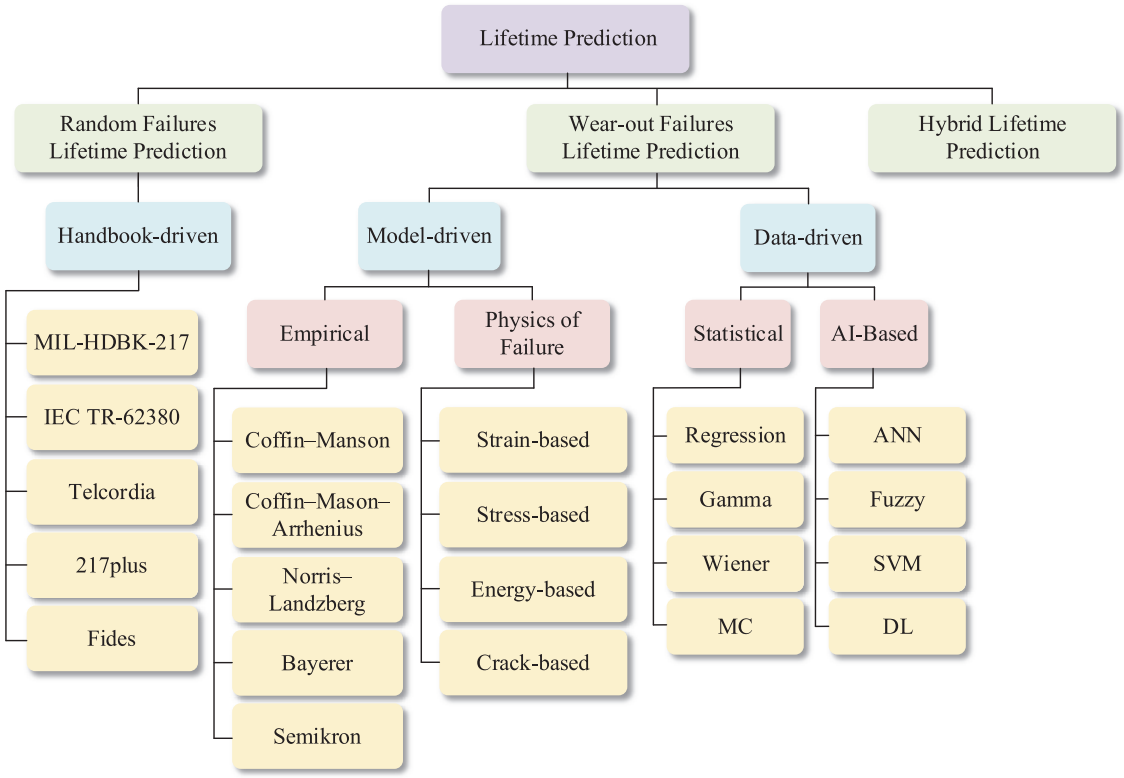

FIGURE 11. Classification of lifetime prediction methods.

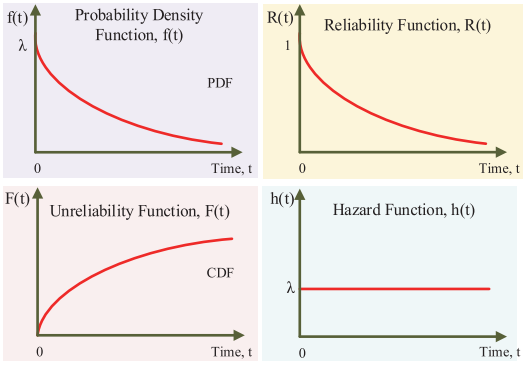

FIGURE 12. Exponential distributions of reliability for random failures.

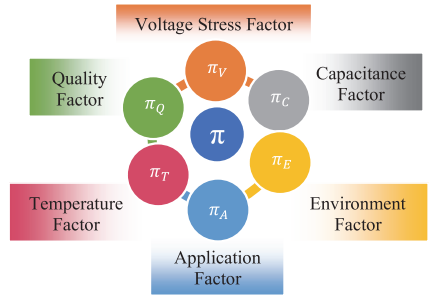

FIGURE 13. Failure parameters diagram.

For capacitor:

$$\lambda_{Capacitor} = \lambda_b \times \pi_T \times \pi_V \times \pi_C \times \pi_Q \times \pi_E \tag{8}$$

The overall converter's failure rate can be calculated as:

$$\lambda = \sum_{i=1}^{n} N_i \pi_{Qi} \lambda_{bi} \tag{9}$$

where, n is the number of parts categories (e.g. MOSFET, capacitor, diodes, etc.), N_i is quantity of i_{th} part, π_{Qi} is the quality factor of i_{th} part, λ_{bi} is the base failure rate of i_{th} part. The π-factors vary for component types and categories.

Later on, International Electrotechnical Commission (IEC) released the IEC TR-62380 handbook, also called RDF 2000, which takes into account the failure mechanisms for calculating the failure rate throughout a mission profile. IEC TR-62380 considers the mission profile for constant failure

rate prediction, but not for the wear-out prediction. Thus, the calculated lifetime may not be precise enough for different operating conditions [58]. As the provided data of this handbook was not updated and the failure mechanisms were not accurately modeled, it has been replaced by IEC 61709, which provides a general guideline for mission profile-based failure rate estimation.

Having faced the problems associated with the military handbook methods, Bellcore telecommunications company decided to design its own reliability prediction standard for its commercial telecommunication products. In 1997, the company's name was changed to Telcordia. Telcordia Issue 3 is a widely used reliability prediction standard, while Telcordia SR-332 Issue 4 represents the latest Telcordia standard. Three methods are used in the Bellcore/Telcordia standard for dealing with failure rates at both the infant mortality stage and the steady-state stage. The first method is similar to the MIL-HDBK-217F standard method which utilizes the generic failure rate along with the device quality factor (π_Q), voltage stress factor (π_V) and temperature stress factor (π_T). In the second scheme, test data are combined with the first method based on specific SR-332 criteria, while in the third scheme, failure rates are estimated by applying a statistical model. Using this method, the predicted failure rate is calculated by taking the weighted average of the generic steady-state failure rate and the field failure rate. Telcordia is a popular reliability assessment approach in the commercial sector. Nonetheless, its use has continued to grow throughout a wide variety of industries.

Quanterion Solutions Incorporated developed the reliability prediction standard 217Plus in 2015, which was released initially as PRISM. A wide range of electromechanical components is taken into account in the failure rate models in 217Plus, which have their roots in MIL-HDBK-217. This standard supports all aspects of a handbook-driven approach including detailed stress calculations, parts count calculations, operating profiles, cycling factors, and process grades. In 217Plus, the Part Count section provides tables describing the device failure rates as a function of the system environment and operation profile. The Part Count section of 217Plus includes a number of tables for device failure rates that are based on the combination of the system's operating profile and environmental factors. It will be possible in this case to obtain the device failure rates by using a table lookup instead of calculating.

$$\lambda = \sum_{i=1}^{n} N_i \sum_{j=1}^{m} \Pi_{ij} \lambda_{ij} \tag{10}$$

where, n is the number of parts categories, N_i is quantity of i_{th} part, m is the number of failure mechanisms appropriate for the i_{th} part category, π_{ij} is π-factor for the i_{th} part category and jth failure mechanism, λ_{ij} is failure rate for the i_{th} part category and j_{th} failure mechanism [66].

Fides approach takes into account failures that are derived from development or manufacturing errors and overstresses such as electrical, thermal, and mechanical. The methodology also deals with non-functioning phases such as dormant application and genuine storage [67]. The evaluation method of FIDES does not consider infant mortality and the wear-out periods of the components except for some special cases for some sub-assemblies [67].

$$\lambda = \Pi_{PM} \Pi_{\mathrm{Pr}ocess} \lambda_{Phy} \tag{11}$$

where Π_{PM} is the quality and technical control over manufacturing of the item, $\Pi_{Process}$ comprises all the steps of item processes from specification to field operation and maintenance, and λ_{Phy} is the quality and technical control over manufacturing is the physical failure rate of the item, which can be calculated in the mission profile phase as:

$$\lambda_{Phy} = \sum_{i}^{Phases} \left[\frac{t_{annual}}{8760} \right]_i \times (\lambda_i \Pi_i) \times \Pi_{Induced,i} \tag{12}$$

where annual is the phase duration in hours during the year. The factor $\Pi_{induced,i}$ is the induced stress factor, which includes electrical, mechanical, or thermal stresses as:

$$\Pi_{Induced,i} = \left(\Pi_{Placement} \Pi_{App} \Pi_{Rugg} \right)^{0.511 \times \ln(C_{sensitivity})} \tag{13}$$

where $\Pi_{\mathrm{Placement}}$ denotes the effect of the item placement in the system, Π_{App} represents the influence of the usage environment for the application of the product contacting the item, Π_{Rugg} represents the influence of the policy for taking account of overstresses in product development. The calculation is explained in [68] but if it is not evaluated, a default value of 1.7 is suggested with reduction in the accuracy of the final result. and $\mathrm{C_{sensitivity}}$ is the sensitivity of the item to over stress.

Wear-Out Failures' Lifetime Prediction: In comparison with random failures lifetime prediction methods, wear-out failures' prediction is typically more complicated with more steps to calculate the reliability. The diagram in Fig. 14, demonstrates the different steps of a typical wear-out failure prediction process. The first step to do so is collecting the failure data including at least one from mission-profile data, test data, and field data. If using the mission-profile data, the next step would be the translation of this data to the thermal profile using electrothermal modeling. After the cycle counting process, a proper lifetime model should be chosen to provide the number of failures per cycle. The deviation of the output parameters after the damage accumulation is estimated to give a precise result. Lifetime distribution results in reliability are demonstrated by either CDF or PDF.

a: ELECTROTHERMAL MODELING

The fundamental step in the mission profile based reliability prediction is translating the converter's mission profile to the corresponding stresses in its prone-to-failure components [72]. Fig. 15 shows the three steps to translate the mission profile in order to achieve the junction temperature change. The first step in extracting the temperature profile from the

TABLE 3. Summary of major handbook standards.

	MIL-HDBK-217 [64]	IEC TR-62380 [69]	Telcordia [70]	217plus [71]	FIDES [68]
Last Update	1995	2016	2006	2015	2009
Operation profile	NO	Yes	NO	Yes	Yes
Thermal cycling	NO	Yes	NO	Yes	Yes
Thermal rise in part	Yes	Yes	NO	Yes	Yes
Solder joints failures	NO	Yes	NO	Yes	Yes
Induced failures	NO	NO	NO	Yes	Yes
Failure rate data base for other parts	limited	limited	NO	Yes	Yes
Infant mortality	NO	Yes	NO	Yes	NO
Dormant failure rate	NO	NO	NO	Yes	Yes
Test data integration	Yes	Yes	NO	Yes	NO
Bayesian analysis	NO	NO	NO	Yes	NO

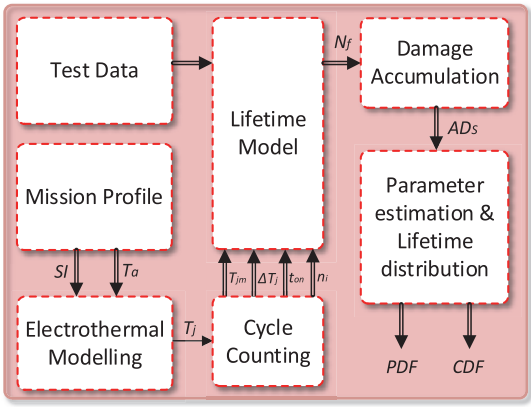

FIGURE 14. General diagram of a typical component-level lifetime prediction process.

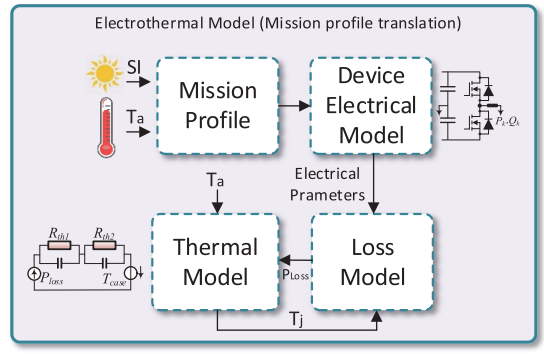

FIGURE 15. General diagram of a typical electrothermal model.

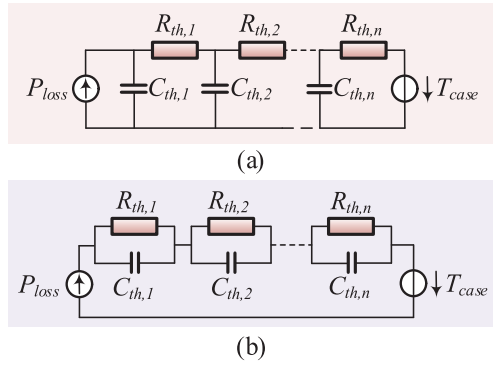

FIGURE 16. Thermal models: (a) Cauer model, (b) Foster model.

mission profile is deriving the electrical parameters from it by using the mechanical system, electrical system, and controller. Extracted electrical parameters are used to calculate the losses in the switches and diodes using the loss model. The thermal model is used to extract the thermal loading or junction temperature from the power losses. The Cauer model or Foster model can be used as the thermal model as shown in Figs. 16(a) and 16(b) respectively [73]. A mix of both Cauer and Foster thermal models is presented in [74], which addresses the shortcomings of the two mentioned models. Using this process, the junction temperature of the power device is obtained.

b: CYCLE COUNTING

The lifetime of a power converter is associated with the magnitude and frequency of the temperature cycles. Each cycle applies different stresses to the module and resulting in a particular consumed lifetime. By using cycle counting, lengthy irregular load-versus-time histories are summarized by providing the number of times cycles of various sizes [50]. Parameters of cycle counting including input parameter T_j

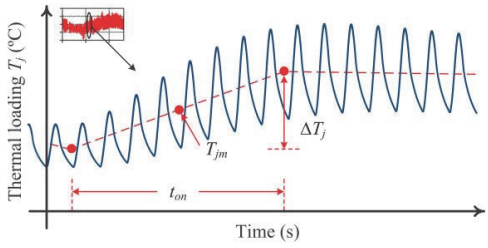

FIGURE 17. Thermal loading parameters.

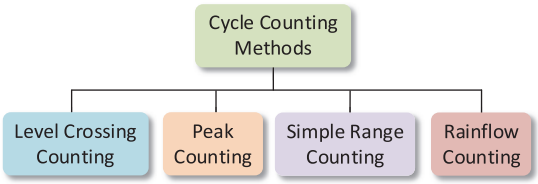

FIGURE 18. Methods of cycle counting.

and output parameters T_{jm}, ΔT_{j}, t_{on} are demonstrated in Fig. 17. The definition of a cycle varies with the method of cycle counting. Several cycle counting methods have been developed for lifetime prediction three of which are level crossing counting, peak counting, range counting, and the rainflow counting (Fig. 18) [42], [75].

In the level crossing counting technique (Fig. 19(a)), one count is recorded each time the positively sloped portion of the load exceeds a preset level above the reference load, and each time the negative sloped portion of the load exceeds a preset level below the reference load. Reference load crossings are counted on the positively sloped portion of the loading history. There is no difference in counting whether positive or negative slope crossings. The distinction is provided only to reduce the total number of events by a factor of two.

Peak counting (Fig. 19(b)) identifies the maximum or minimum load value. Peaks above the reference load level along with the valleys below the reference load level are counted. A modified version of his method can be obtained by counting all peaks and valleys disregarding the reference load [76].

The range counting method considers the difference between two successive reversals as a range. When a valley is followed by a peak, the range is positive, while when a peak is followed by a valley, the range is negative (Fig. 19(c)).

In the rainflow counting method (Fig. 19(d))., the first step is to rotate the loading history by 90 degrees such that the time axis is vertically downward. By imagining a flow of rain starting at each successive extremum point a loading reversal (half-cycle) is defined by allowing each rainflow to continue to drip down these roofs until it falls opposite a larger maximum or smaller minimum point, meets a previous flow falling from above and falls below the roof. By pairing

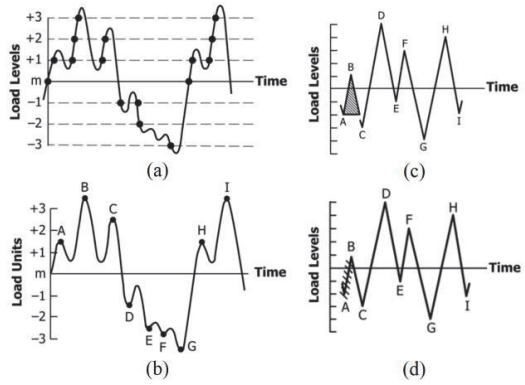

FIGURE 19. Load-time diagrams of different cycle counting methods.

up the same counted reversals, hysteresis loops (cycles) can be identified. In the rainflow counting approach, a large data storage system is required since it only processes the data in chunks which is inconvenient to implement in a real-time application. To address this issue, a real-time rainflow counting technique is proposed in [43] which uses a recursive algorithm.

c: LIFETIME MODEL

Handbook-driven approaches benefit from the straightforward failure rate calculation, however, all the aforementioned handbook approaches carry some shortcomings despite having updates on their handbooks [77].

Model-based approaches offer better accuracy since the failure rates are calculated based on the results of the real-life accelerated test results and actual physics of the components and their failure modes and mechanisms along with the effect of stresses of the product-level on the reliability of the components. There are also data-driven methods in which models are typically "black boxes" with no explicit system knowledge. Data-driven approaches involve learning statistical relationships and patterns from the failure data to provide valuable decision-making information.

i) MODEL-DRIVEN LIFETIME MODELS

Model-driven lifetime models describe degradation processes through building mathematical models based on accelerated tests using parameterization as empirical methods or based on the failure mechanisms and materials as PoF methods [23]. In theory, all model-based lifetime models have some parameters to be determined and module geometry and material properties are necessary to determine the unknown parameters. Therefore, as some PoF models need parameterization, there no definite borderline between empirical and PoF models.

ii) EMPIRICAL MODELS

Empirical models are deduced from experience and large databases of accelerated aging experimental data collected

over many years for different module technologies. The accuracy of such models can only be guaranteed when used in situations similar to the test conditions from where the models were "born" [29]. They express lifetime in terms of the number of cycles to failure, N_f. These models describe the N_f-dependence on the parameters of accelerated tests, such as maximum, mean, or minimum temperature, cycle frequency, heating and cooling times, load current, and the power module's properties such as blocking voltage class, and the geometry of bond wires.

Coffin–Manson model is the most widely used approach among the empirical analytical modeling methods [78]. It describes the effect of the junction temperature fluctuation ΔT_j. In this case, the lifetime is inversely proportional to the temperature swing [79].

$$N_f = A \times \left(\Delta T_j\right)^{-\alpha} \tag{14}$$

where A and α are the curve fitting parameters which can be fitted using simulation or a cyclic experiment.

The Coffin–Manson model can be enhanced to provide another model by adding the effect of the mean junction temperature T_{jm} known as Coffin–Mason–Arrhenius model, where K_b is the Boltzmann constant and E_A is the activation energy parameter. It is given as [31]:

$$N_f = A \times \left(\Delta T_j\right)^{-\alpha} \times \exp\left(\frac{E_a}{K_b \times T_{jm}}\right) \tag{15}$$

Nevertheless, this model does not consider the cycle heating time, which strongly affects the bond wire fatigue. The Norris–Landzberg model takes into account the cycling frequency (f) of the junction temperature, where the β is a curve fitting parameter [31], [80].

$$N_f = A \times f^{\beta} \times \left(\Delta T_j\right)^{-\alpha} \times \exp\left(\frac{E_a}{K_b \times T_{jm}}\right) \tag{16}$$

Bayerer model utilizes a large number of parameters and considers more detailed information derived from the power cycling tests and power module characteristics which makes this approach more complicated than the aforementioned techniques. In this approach, two dominant failure mechanisms have been taken into account: bond wires lift-off and baseplate solder failure. Eq. 17 defines the formula of this model where T_{jm} is the maximum junction temperature, t_{on} is the heating time, V is the blocking voltage, I is the applied dc current, D is the diameter of the bond wire, and the β constants are fitting parameters [81].

$$N_f = A \times \left(\Delta T_j\right)^{\beta_1} \times \exp\left(\frac{\beta_2}{T_{j\max}}\right) \times t_{on}^{\beta_3} \times I_{DC}^{\beta_4} \times V_{block}^{\beta_5} \times D^{\beta_6} \tag{17}$$

Semikron model is defined for the advanced power modules with sintered chips in which the soldering process for the die attach is replaced by Ag-diffusion sintering technology. In this model, the bond wire lift-off and heel cracking are the only observed failure modes, so that the developed lifetime model corresponds only to the failure mechanisms due to thermo-mechanical stress of bond wires [82], [83].

$$N_f = A \times \left(\Delta T_j\right)^{\alpha} \times ar^{\beta_1 . \Delta T_j + \beta_0} \times \left(\frac{C + t_{on}^{\gamma}}{C+1}\right) \times e^{\frac{E_a}{k_b . T_{jm}}} \times f_{Diode} \tag{18}$$

where f_{Diode} is a derating factor applied for the test on free-wheeling diodes, ar is the aspect ratio of Al bond wire; β_1 and β_2 are the model coefficients determined together with the other model parameters A, α, C, γ, E_a, and f_{Diode}, using a least square fitting procedure.

TABLE 4. Model parameters and variables of empirical methods.

Eq.	Lifetime Model	Model Parameters	Variable Considered
(13)	Coffin–Manson	A, α	ΔT
(14)	Coffin–Mason–Arrhenius	A, α, E_a	$\Delta T_j, T_m$
(15)	Norris–Landzberg	A, α, β, E_a	$\Delta T_j, T_m, f$
(16)	Bayerer	A, α, β, E_a	$\Delta T_j, T_{jm}, t_{on}, I_{DC}, V_{block}, D$
(17)	Semikron	$A, \alpha, \beta, C, \gamma, E_a, f_{Diode}$	$\Delta T_j, T_{jm}, t_{on},$

iii) PoF MODELS

Since empirical models lack the description of physical structures of power devices and the actual failure mechanisms, such as the crack propagation of solder layers, some researchers have begun to focus on the POF models of power devices. In this approach, the assessment of a component is done based on investigating the real physics behind the root failure mechanisms, and the impact of stress profiles, manufacturing technologies, and materials are taken into consideration along with any other factor that might affect the product's Remaining Useful Lifetime (RUL) [29]. Different from the empirical models, the PoF models need to know the failure mechanisms and the deformation mechanisms of power devices in advance so that the stress and strain development within the power module assembly is modeled and directly correlated to the number of cycles to failure.

There are two ways of measuring the stress and strain in electronic packages: One way is direct measurements which demands the usage of high-resolution measuring methods, and the other way is through the stress analysis of materials by experiments or Finite Element Analysis (FEA).

Strain-based models assumes that plastic strain is the main cause of the bond wire lift-off and emphasize on the effects of plastic strain as follows [84]:

$$N_f = C_1 \times \left(\Delta \varepsilon_p\right)^{-C_2} \tag{19}$$

where $\Delta \varepsilon_P$ is the average accumulated plastic strain per cycle and C_1 and C_2 are material-specific parameters.

By adding the effect of solder fatigue, Eq. (20) will be obtained:

$$N_f = \frac{L}{a \times \left(\Delta\varepsilon_p\right)^b} \tag{20}$$

where L is the length of the solder interconnect and a and b are material-dependent constants.

Stress-based model uses the Basquin equation to describe the damage induced by stress range [85]:

$$N_f = C_1 \times (\Delta\sigma)^{-C_2} \tag{21}$$

where $\Delta\sigma$ is the stress range and C_1 and C_2 are material-specific parameters.

Energy-based approach is consider both stress and strain and are based on the strain–stress hysteresis energy as follows [86]:

$$N_f = \frac{E_f}{E_c} \tag{22}$$

where E_f is the total energy to failure and E_c is the energy per cycle.

Crack-based models are based on the crack propagation within the assembly of a chip soldered on a copper substrate which can be characterized by scanning acoustic microscopy, measurements of the thermal resistance, and FEM for predicting the crack initiation and propagation using the Paris law [87].

$$\begin{aligned} N_0 &= C_1 \times (\varepsilon_a)^{C_2} \\ \frac{da}{dN} &= C_3 \times (\varepsilon_a)^{C_4} \end{aligned} \tag{23}$$

where ε_a is the mean value of the integrated accumulated creep strain along the lines coinciding with the direction of the crack propagation, N_0 is the number of cycles until crack initiation, da/dN is the crack propagation rate, and the constant parameters C_1, C_2, C_3, *and* C_4 are the material-dependent coefficients, which are determined by means of FEM simulations.

iv) DATA-DRIVEN MODELS

The data-driven methods require less complexity in prediction compared with PoF techniques. The benefit of the remaining time and energy can be used in designing and verification of the algorithm. In this method, the model is built based on the operational data of different periods derived from a large number of experiments [41].

Generally, the data-driven methods fall into two categories: The statistical approaches including Gaussian Process Regression (GPR), the gamma process, the Wiener process, hidden Markov Chains model (MC). There is also Artificial Intelligence (AI) approaches that include Artificial Neural Network (ANN), fuzzy logic, Support Vector Machine (SVM), and Deep Learning (DP). Among these algorithms, ANN and GPR are the most used data-driven approaches [88].

Regression-based models are the most commonly used statistical data-driven techniques. The GPR method is based on the idea that the higher the similarity of two inputs, the stronger the correlation of the corresponding outputs. It assumes that both predicted and historical parameters follow the multi-dimensional joint Gaussian distribution, and the marginal distribution of the predicted parameter can be obtained using the calculation of the covariance matrix [89]. GPR shows good adaptability in high dimensional, small-sample learning problems as well as nonlinear prediction problems. In addition, it benefits from less adjustable parameters and strong interpretability high computation needed in this approach can be seen as a drawback. Modeling through the Wiener process or Brownian motion with drift is suitable when the degradation develops bidirectionally over time with Gaussian noises. Gamma process models are applied in cases in which the occurrence of the degradation is gradual over time in a sequence of small positive increments. These models take the advantage of having relatively straightforward mathematical calculations along with taking into consideration the temporal variability.

AI modeling methods help reduce the computational burden and the need to store huge loads of lifetime data [90]. Fig. 21 shows all possible machine learning approaches some of which have been used in the reliability assessment of power electronic systems and other techniques have the potential to further be investigated in this field.

One group of AI approaches are neural network methods three of which are Feed Forward Neural Network (FNN), Recurrent Neural Network (RNN), and Convolution Neural Network (CNN). FNN is the fundamental form of neural network which maps the input to output in a forward direction. Another form of Neural Network is RNN which is designed to recognize sequences. This technique has been extended across time by having edges feeding into the next time step instead of into the next layer in the same time step. The third neural network approach is CNN which is based on recognizing images using convolutions inside to identify the edges of an object on the images [91]. For data analysis, FNN is much more suitable, while RNN and CNN are mostly used in the processing and recognition of images, texts, audio, videos, etc., where sequence and spatial features are the important factors.

In the ANN approach in [92], the first step is providing the lifetime data associated with operating conditions using electro-thermal models and stress-strength analysis. As a result, a set of limited lifetime data (L_i) attributed to the active and reactive powers (P_i, Q_i) is generated. In the case of using the data of the manufacturer, providing electro-thermal and lifetime models is not needed which might be confidential in most cases. In the second step, the generated lifetime data is utilized to train the ANN network depicted in Fig. 20. The input for the next layer is generated by processing the information from the neurons of the preceding layer. Thus, the performance index is provided by ANN employing the limited lifetime data.

The final step consists of classifying the active and reactive power profiles and presenting their frequency by a Probability

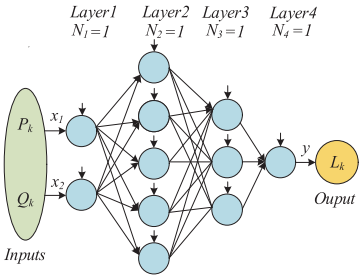

FIGURE 20. Sample ANN structure.

Mass Function (PMF). The converter lifetime associated with each pair of P_i and Q_i is obtained using the performance index curves provided in the third step or predicted by using the ANN trained in the second step. Therefore, the B_n lifetime under a given mission profile can be predicted as Eq. 24, where F_i is the frequency of the active and reactive powers:

$$L(B_n) = \left(\sum F_i/L_i\right)^{-1} \tag{24}$$

A time-delay failure model using ANN is used in [93] in combination with the probabilistic function by utilizing the maximum likelihood technique for IGBT model optimization. In [94], a recurrent neural network approach is employed in the prognostics of the system [88].

In the SVM technique, which is a supervised machine learning method based on classification, structural risk minimization is used instead of empirical risk minimization. It solves the typical ANN problems associated with prediction and classification, non-linear functions, and loss functions. SVM finds a line/hyperplane in multidimensional space to separate the classes and classifies the new data depending on whether it lies on the positive or negative side of the hyperplane depends on the classes to predict [95].

Support Vector Regression (SVR) is another supervised machine learning technique similar to SVM but with the difference that it is based on regression rather than classification [96], [97].

In [98], a deep learning approach is used combined with edge and cloud computing technologies to enable a real-time precise reliability modeling of high-frequency power converter devices. It is based on stacked long short-term memory for collective reliability training and inference across collective MOSFET converters by detecting the change in the drain-source resistance.

d: DAMAGE ACCUMULATION

After the damage caused by each thermal cycle is determined, the total accumulation of damage is calculated, and an initial estimation of the device's lifetime can then be obtained by either linear or nonlinear means [99]. One of the commonly used methods in damage accumulation evaluation is the Palmgren-Miner law [81]. The formula for calculating the damage accumulation by this method is as follows:

$$D = \sum_{i=0}^{N} \frac{n_i}{N_i} \tag{25}$$

where D stands for accumulated damage, N stands for the total number of power cycles generated by the rainflow counting algorithm, n_i is the number of cycles for i^{th} power cycle, N_i is the number of cycles to failure at the corresponding ΔT_j and T_m in the i^{th} power cycle [56].

However, this approach has some limitations including considering the damage accumulation rate constant during the lifetime along with being independent of the loading levels leading to reduced lifetime prediction accuracy. More damage would increase the stresses which cause additional physical mechanisms resulting in a different damage accumulation rate [100]. For instance, when the crack propagates, as a result of increased power loss, thermal resistance increases which leads to an accelerated damage accumulation rate in bond wires and solder layers. Hence, the predicted lifetime using linear methods would be impractically longer.

The nonlinear damage accumulation approach reflects the accumulation rate change in different stress levels. A technique based on the double linear damage law analyzes each phase of the loading using the Palmgren-Miner linear damage method. However, it does not take into account the mutual interaction among different stresses [34], [101]. Manson–Halford model addresses this issue by considering both stress sequences and interaction by changing the exponent parameter in the double linear damage model [102], [103]. There are nonlinear approaches that take into account the damage accumulation rate change by placing proper weights onto the affected physical parameters. As detailed experimental data are needed to determine these weights, these techniques are not applied much [34].

Fatemi and Yang [104] in 1998 published a very comprehensive review that categorized cumulative damage models in six categories: (a) linear damage rules, (b) nonlinear damage curve and two-stage linearization methods, (c) life curve modification methods, (d) approaches based on crack growth concepts, (e) continuum damage mechanics models, and (f) energy-based theories. As one of the recent reviews, [105] has reviewed cumulative damage models for high-cycle fatigue.

e: PARAMETER ESTIMATION AND LIFETIME DISTRIBUTION

The basic idea of parameter estimation is modeling the parameters used in the calculation (e.g., stress parameters in a lifetime model) using a certain distribution function ($f(x)$), instead of fixed parameters [50] with a range of variations (e.g., normal distribution with 5% parameter variation). In this way, the parameter variations can be introduced in the calculation to represent uncertainties in practical applications. Then, the lifetime evaluation is carried out with a set of n samples. By doing so, the lifetime distribution (e.g., the

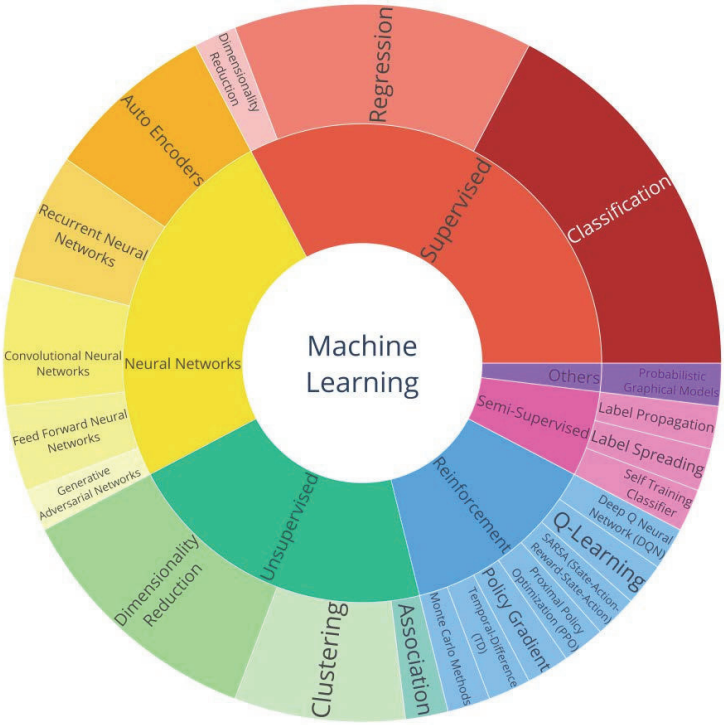

FIGURE 21. Various methods of machine learning [112].

Weibull distribution) of a power electronic component can be constructed from the lifetime yield of n samples [106].

Different distribution methods are defined in Table 5. Weibull distribution is the most popular distribution in lifetime prediction. In this method, the shape parameter β represents the failure mode of the component, where the components that have experienced the same failure mode/mechanism will have similar shape parameter β [107].

Monte Carlo simulations are widely used for analyzing the stochastic behavior of model parameters, which represents uncertainty in the prediction [7]. The Monte Carlo method is based on simulating the model parameters with a certain distribution, representing variation, and randomly selecting them during each simulation [108]. In the next step, if the number of simulations is large enough, the simulation results are expected to converge to the expected value, based on the law of large numbers [109]. In this case, the Monte Carlo simulation (with a large number of simulations) will thus result in a distribution indicating the probability of each of the possible outcomes [110].

After that, the PDF is obtained using a distribution in Table. 5. From the lifetime distribution of the component it is also possible to obtain the component unreliability function $F(x)$, which is the CDF of the distribution (Fig. 22) [111]. The unreliability function can be used to indicate the development of failure overtime. For instance, the time when $x\%$ of the components failed can be obtained from the unreliability function, and it is normally referred to as the Bx lifetime (Fig. 22(b)) [50].

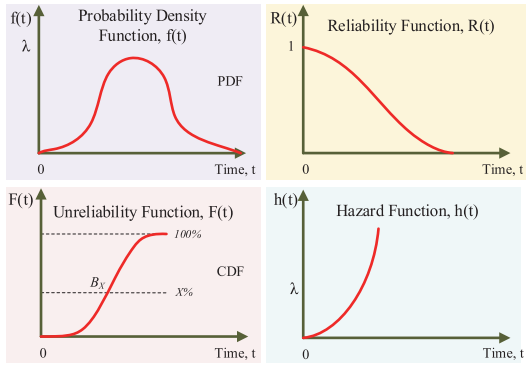

FIGURE 22. Weibull distributions of reliability for wear-out failures.

Comparison of Lifetime Prediction Methods: Lifetime prediction methods are compared in Table 6 mentioning their advantages and disadvantages. Handbook-driven lifetime prediction approaches benefit from the simplicity of usage and using the real field data. However, they are considered to be inaccurate, especially in the presence of new

TABLE 5. PDF and CDF formulas for different distributions [54], [113], [114].

Distribution		CDF	PDF
Uniform		$F(t)=\begin{cases}\frac{t-a}{b-a} & a\le t\le b\\ 0 & Otherwise\end{cases}$	$f(x)=\begin{cases}\frac{1}{b-a} & a\le x\le b\\ 0 & Otherwise\end{cases}$
Triangular		$F(t)=\begin{cases}\frac{(t-a)^2}{(b-a)(c-a)} & a\le t\le c\\ 1-\frac{(b-t)^2}{(b-a)(b-c)} & c\le t\le b\end{cases}$	$f(t)=\begin{cases}\frac{2(t-a)}{(b-a)(c-a)} & a\le t\le c\\ \frac{2(b-t)}{(b-a)(b-c)} & c\le t\le b\end{cases}$
Normal		$F(t)=\Phi\left(\frac{t-\mu}{\sigma}\right)$	$f(t)=\frac{1}{\sigma\sqrt{2\pi}}\exp\left(-\frac{1}{2}\left(\frac{t-\mu}{\sigma}\right)^2\right)$
Lognormal		$F(t)=\Phi\left(\frac{\ln t-\mu}{\sigma}\right)$	$f(t)=\frac{1}{t\sigma\sqrt{2\pi}}\exp\left(-\frac{(\ln(t)-\mu)^2}{2\sigma^2}\right)$
Weibull	2 Parameters	$F(t)=1-e^{-\left(\frac{t}{\eta}\right)^{\beta}}$	$f(t)=\frac{\beta t^{\beta-1}}{\eta^{\beta}}e^{-\left(\frac{t}{\eta}\right)^{\beta}}$
	3 Parameters	$F(t)=1-e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}}$	$f(t)=\frac{\beta(t-\gamma)^{\beta-1}}{\eta^{\beta}}e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}}$
Extreme Value	Min	$F(t)=1-\exp\left(-\exp\left(\frac{t-\eta}{\sigma}\right)\right)$	$f(t)=\left(\frac{1}{\sigma}\right)\exp\left(-\exp\left(\frac{t-\mu}{\sigma}\right)\right)\left(1-\exp\left(-\exp\left(-\frac{t-\mu}{\sigma}\right)\right)\right)$
	Max	$F(t)=\exp\left(-\exp\left(\frac{t-\eta}{\sigma}\right)\right)$	$f(t)=\left(\frac{1}{\sigma}\right)\exp\left(-\exp\left(\frac{t-\mu}{\sigma}\right)\right)\exp\left(-\exp\left(-\frac{t-\mu}{\sigma}\right)\right)$

TABLE 6. Summary of advantages and disadvantages of various component-level lifetime prediction methods.

Method	Advantages	Disadvantages
Handbook-driven	✓ Reflects actual field failure rates and defect densities ✓ Simplicity of usage ✓ Can be a good indicator of field reliability	☒ Difficult to keep up to date ☒ Difficult to collect good-quality field data ☒ Difficult to distinguish cause vs effect for the correlated variables (e.g., quality vs environment).
Model-driven	✓ Modeling of specific failure mechanisms ✓ Explicitly considers the impact of design, manufacturing, and operation on the end-of-life	☒ Cannot be used to estimate field reliability ☒ High complex and expensive to apply ☒ Cannot be used to model defect-driven failures
Data-driven	✓ Reflects the actual reliability ✓ Test data can be collected and applied before the system is deployed	☒ Translations to field stresses are required, which requires acceleration models and adds uncertainty to the estimate

approaches that precisely take into account the wear-out phase of the components and systems.

The main drawback of the PoF lifetime model is the complexity of usage since a deep understanding of the root mechanisms of the failures is needed. However, it has features making it a proper approach for reliability assessment as it explicitly considers the impact of design, manufacturing, and operation on the end-of-life of the products [115].

Data-driven modeling has shown a number of key advantages over its physics-based counterpart, such as substantially reducing the expertise required to use the models.

2) HYBRID LIFETIME PREDICTION

The hybrid models combine at least two of the lifetime prediction methods as shown in Fig. 23 [116]. As an example, [117] combines handbook-driven assessment using MIL-HDBK-217 handbook and model-based method using Coffin-Manson-Arrhenius model in order to take into account both models along with IEC 62380 handbook. Using a hybrid method provides a more precise and comprehensive lifetime prediction and makes it possible to benefit from the merits of each technique and overcome its deficiencies.

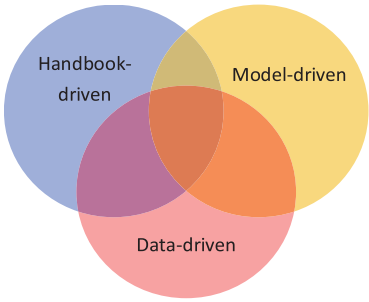

FIGURE 23. Venn diagram of three lifetime prediction methods to create hybrid methods.

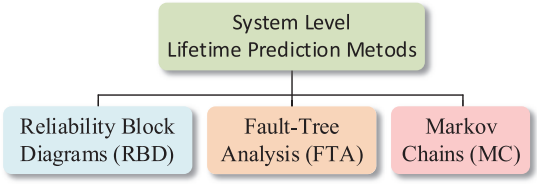

FIGURE 24. System-level lifetime prediction methods.

B. SYSTEM LEVEL LIFETIME PREDICTION

Various methods are used to map the reliability of the components to the systems, including Reliability Block Diagrams (RBD), Fault-Tree Analysis (FTA), and Markov Chains (MC) [118], as shown in Fig. 24.

RBD models the impact of a failure on the system, without necessarily modeling the mechanical structure. Therefore, in this method, the failure of components that are physically present only once in the system may occur at several locations. Fig. 25(a) demonstrates the typical series and parallel RBD diagrams in which the node I is the input and the node O is the output. The system functions whenever there is a path between the input and output nodes formed by the functioning components, otherwise, the system fails [119].

FTA is an analytical technique that applies a top-down approach to analyze the various system combinations of hardware, software, and human failures as sub-events that may cause the system failure as the top event [37], [120]. This method classifies the events as initiating fault events, intermediate events, and top events and uses logic gates such as AND, OR, etc., to transform the component-level lifetime data to the system-level (Fig 26(b)) [19], [25], [61].

MC is a state space analysis method that assumes that the future behavior of the system depends only on the current state and the system is memoryless. Fig. 25(c) depicts a typical MC with three states in which $P(i, j)$ is the transition probability [121]. Compared to the other system-level approaches, MC is well suited to modeling additional system states introduced by fault-tolerance or redundancy, along with the maintenance and repair process. For instance, a simple fault-tolerant system may consist of three states, including the healthy state, the failure state, and the post-fault state. The healthy and postfault states are both considered as operational states [77]. The MC approach can be simulated as a state space system, in which the state variables are the probabilities that a system will reach each state over time [122].

The state matrix can be provided using the Markov transition rates $P(i, j)$, which in the case of modeling the reliability they can be the summation of the failure rates [25]. The reliability assessment of several dc-dc converters has been done using MC in [60], [122], [123], [124], and [125].

System-level lifetime prediction methods are summarized in Table 7 indicating the elements used in these approaches along with the merits and drawbacks of each technique.

IV. LIFETIME EXTENSION

Although lifetime analysis and prediction are important and fundamental steps of achieving high reliability, performing them is not enough to achieve reliable products. There is a set of other activities involved in an effective reliability plan to achieve reliable products. Achieving a product's reliability goals requires a strategic vision to use a design process that insures reliability. The necessity of taking the advantage of a proper condition monitoring procedure as an efficient, non-intrusive process that has the potential to prevent production loss and guarantee long-term productivity, is inevitable.

A. RELIABLE DESIGN

During the early development stages of the product, reliability analysis tools are used to ensure that the product design meets specific lifetime and safety criteria. Typically, after several design iterations, and only after the reliability requirements have been met, the product can move forward toward more mature product lifecycle stages [126].

1) DESIGN FOR RELIABILITY (DfR)

Design for X (DfX) is a design guideline that proposes an approach with its corresponding methods that may help to provide and apply technical knowledge to control and improve a particular feature of a product [127]. Currently, around 50 different DfX approaches have been proposed and explored in extensive papers by industry experts. DfX approaches can be developed around any feature that is critical to the product and its manufacturer or the organization.

By considering reliability in DfX as an important feature of every product, DfR is obtained. DfR describes a comprehensive set of tools that help to support product and process design from early on in the conception stage through to the point of obsolescence. As a result of this process, the customer can expect full customer satisfaction throughout the life of the product with low overall life-cycle costs [22]. To put it simply, DfR is a systematic, streamlined, concurrent engineering program that incorporates reliability engineering into the design process. To accomplish this, reliability engineering tools must be properly used in conjunction with an understanding of when and how to use them throughout the development cycles. A manufacturer must follow this process

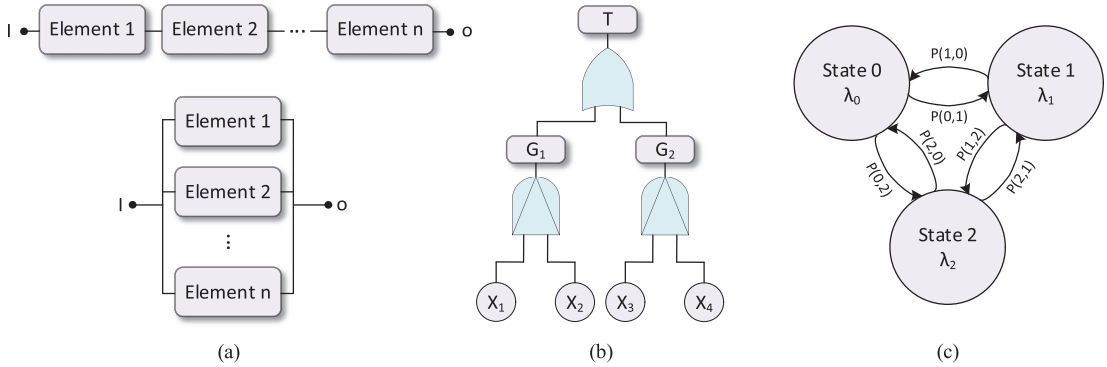

FIGURE 25. Sample diagrams of different system-level lifetime prediction methods. (a) RBD, (b) FTA, (c) MC.

TABLE 7. Summary of various system-level lifetime prediction methods.

Method	Elements	Advantages & Disadvantages
MC	▪ States ▪ Probability transitions between states ▪ Transition rates	✓ It is dynamic since it represents the state of every component along with the dependences among them at any time. ✓ It can be employed for repairable systems. ☒ A large number of state-based models since the number of states can be 2^n with n components. ☒ Only applied for constant failure and repair rates which neglect the wear-out phase.
RBD	▪ Rectangle blocks ▪ Direction lines ▪ The failure rate of the components or the subsystems represented by each block	✓ Simplicity and ease of use. ☒ Limitations in considering external events such as the human factor and priority of the events. ☒ Inadequacy of the handling of dependencies between components and subsystems.
FTA	▪ Events ▪ Logic gates ▪ Probability of each event	✓ Considering all factors including human factors. ✓ Identifying the failure causes and design problems. ☒ Difficult to manage dependencies among components and subsystems.

in order to benefit from a reliable design of its products as it entails using a wide range of tools and practices [128].

A product fails when the stress experienced by the product exceeds its strength according to the Stress-Strength Interference principle [19]. The interference between stress and strength which is the dashed area in Fig. 26, must be reduced to reduce the failure probability. This goal can be accomplished by means of a structured process, such as the DFR process. Fig. 27 represents a flowchart of a sample DFR process used by Reliasoft and its different stages along with the interactions between them. According to the product type and the amount of information available, the sequence of the activities within the DFR process may differ. While this process is depicted in a linear sequence, in reality, some activities are likely to be performed in parallel or in a loop based on the knowledge gained as the project progresses.

The DfR process can be divided into six main activities to make it general and applicable to varied industries. As shown in Fig. 28, these stages are as follows: 1) Identify, 2) Design, 3) Analyze and Assess, 4) Quantify and Improve, 5) Validate and 6) Monitor and Control [129].

B. CONDITION MONITORING

After designing the power electronic systems, their reliability can be further improved using condition monitoring. The purpose of condition monitoring is to detect a significant

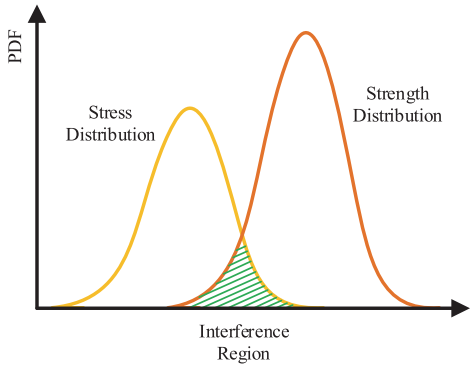

FIGURE 26. Illustration of stress-strength interference.

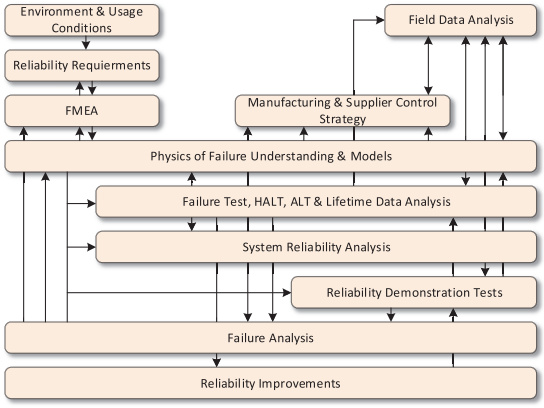

FIGURE 27. Flowchart of a sample DFR process.

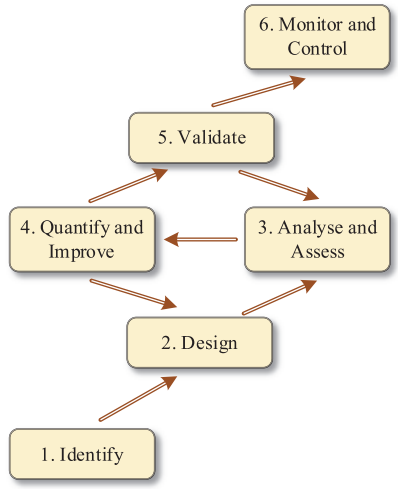

FIGURE 28. General diagram of a typical DFR process.

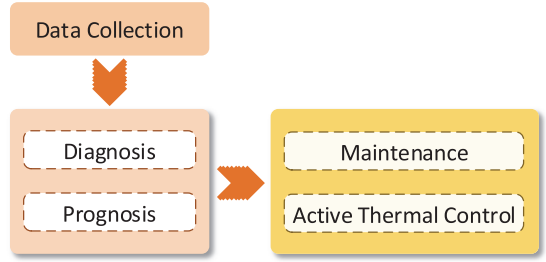

FIGURE 29. General diagram of the condition monitoring process.

change in a parameter such as vibration and temperature with an indication of a developing fault in product [126]. By using condition monitoring, maintenance and other precautions to prevent the failures can be scheduled, in order to minimize the consequences [130]. During the implementation of any control process, monitoring is a crucial function. All the closed loop control approaches rely on the monitoring the output variables of the process. Besides controlling, it is also used to provide information about converter's failure status. The general diagram of condition monitoring is demonstrated in Fig. 29.

1) DIAGNOSTICS

Diagnostics involves determining a problem or fault in a product, system, or component and analyzing the root causes of the problem [64], [69]. It focuses on existing data to diagnose the failure modes and their pattern.

2) PROGNOSTICS

Prognosis is a technique that makes use of the acquired condition monitored data to predict a variety of useful information relating to the condition of the system or the component [35]. It is an estimation technique for the RUL of a product, the probable condition of the device after the specified time, and the probabilities of reliable operations henceforth [130]. The advantage of the prognostic technique is reducing the repair cost and unforeseen failures since at this stage, faults and failures along with the end-of-life of the product are predicted.

3) MAINTENANCE

The term maintenance refers to recurring and regular processes used to keep a unit or component in a healthy and operating condition so that it is capable of producing the expected outcome without degrading service or decreasing component life. There are four types of maintenance approaches in practice as explained in Fig. 30 including reactive maintenance, preventive maintenance, prescriptive maintenance, and predictive maintenance [39].

4) ACTIVE THERMAL CONTROL

By using degradation indicator data from online condition monitoring, a system lifetime can be passively maintained and actively maintained. There are a number of techniques

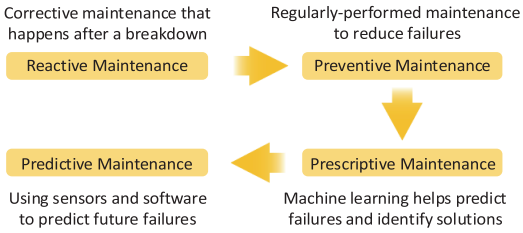

FIGURE 30. Different maintenance methods with arrows showing their evolution direction.

available for component-level active thermal control of power switches, such as switching frequency control, active cooling control, PWM control modification, turn-off delay time control, and hybrid control [131].

V. CONCLUSION

The reliability of power converters can be discussed from two aspects including lifetime management and fault management. The lifetime of power converters is one of the most influential factors on initial investment and economic analysis of a project. If the converters' replacement and maintenance costs exceed the equipment's manufacturing costs, this will generate a negative return on investment.

The first step in the assessing the lifetime of the components, is analyzing the physics of their potential failure mechanisms helps the reliability enhancement efforts to strengthen the lifetime of the converter's stresses caused by temperature increases and abrupt temperature fluctuations are the main mechanisms of failure in power switching devices as one of the main prone-to failure components of converters.

In order to assess the reliability of a converter, handbook-driven methods can be used in the early stages of the design to quickly obtain the lifetime prediction of random failures of power electronic components. However, researchers are shifting away from simple handbook-driven approaches to model-driven and data-driven methods in research on power electronics reliability which consider the wear-out failures. Lifetime prediction of wear-out failures at the component level consists of five steps including electrothermal modeling, cycle counting, lifetime model, damage accumulation, parameter estimation, and lifetime distribution. Among the four cycle counting methods, rainflow counting is considered the best and the most popular method. Model-based lifetime models consider the effect of design, manufacturing, and operation on the end-of-life of the products are considered, while data-driven modeling methods reduce the expertise required to use the PoF models by considering the system as a box without the need for understanding the root failure mechanisms. In model-based lifetime models, since the intrinsic degradation mechanism or empirical knowledge is considered, compared with data-driven methods, model-driven methods can be effective even when the reference data are not sufficient. Using PoF to assess reliability is still an open topic of research, while interactions between different failure mechanisms will make the analysis more complex. The data-driven strategies especially the approaches based on machine learning are to be further studied. Palmgren–Miner's Law is commonly employed in fatigue damage accumulation. It is encouraged to conduct further research on nonlinear damage accumulation techniques such as the Manson–Halford model instead of only considering the linear approaches. Most of the system-level lifetime modeling for converters has been conducted by using an RBD or MC.

Reliability assessment gives us a valuable understanding of how to extend the lifetime of the converter. The fundamental effort to extend the lifetime happens during the design process using reliable design processes such as DfR. Condition monitoring is crucial after the design process to maintain the lifetime which includes data collection, diagnostics, prognostics, maintenance, and active thermal control.

The combined benefits of lifetime prediction and condition monitoring approaches make it easier for companies to choose when to carry out maintenance operations based on cost considerations.

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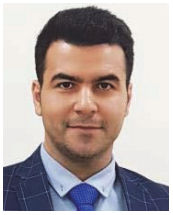

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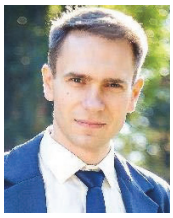

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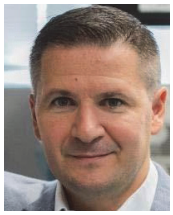

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Design and Analysis of a DC Solid-State Circuit Breaker for Residential Energy Router Application

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Abstract: Energy routers act as an interface between the distribution network and electrical facilities, which meet the requirements of clean energy substitution and achieve the energy sharing and information transmission in the energy network. However, the protection of the dc load side of residential energy routers including interruption and isolation of short-circuit fault currents is vital for discussion. Since the traditional mechanical and hybrid circuit breakers for dc fault protection have the drawback of slow operation, a solid-state circuit breaker (SSCB) is an optimal solution for fast dc fault interruption. In this paper, a dc SSCB is proposed that uses an RCD + MOV snubber circuit, which is considered the best and most complete circuit used in common SSCBs. There are two main contributions in this paper: First, a dc SSCB is designed, which isolates both positive and negative terminals of a circuit and its working principle and operating modes along with the formulas for calculation of crucial time intervals, voltages, and currents along with the design procedure are provided. Second, a soft turn-on auxiliary is designed to prevent a high current surge caused by the capacitance difference between the source and the load. The experimental results demonstrate the proper performance of the topology and the validity of the findings.

Keywords: circuit breaker; solid-state; energy router; dc protection; solid-state circuit breaker; soft turn-on

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1. Introduction

In the last decade, the investigation of different aspects of energy routers has become popular. An energy router is a kind of intelligent power electronics equipment, which can dispatch distributed energy quantitatively, regularly, and accurately [1]. The structure of a typical energy router is shown in Figure 1. As it interfaces various sources and converts the power to ac and dc, an energy router can flexibly manage the dynamic power within the regional power grid on the premise of ensuring power quality [2]. The architectures, functionalities, and demonstration of energy routers have been introduced in [3]. Energy routers play an important role in smart grids since in these grids energy is generated mostly from distributed energy sources [4]. The local loads are powered by these energy resources; however, when the supply of the energy resources surpluses the local demand, the energy flows into the grid through energy routers. The energy router also tracks the variations in the user's demands to distribute the energy dynamically [5–7].

As a critical technique to guarantee the safe operation of the dc side in residential energy routers, a dc circuit breaker is considered as a reliable method of isolating faults in dc systems quickly and selectively [8]. However, since there is no zero-crossing point in the dc current along with a high fault current rising rate, the operation of interrupting the fault current in the dc system is much more difficult compared with the ac system. Therefore, the design of dc circuit breakers becomes crucial, making it a key technology for dc systems [9]. Different kinds of dc SSCBs have been collected and reviewed in [10–14].

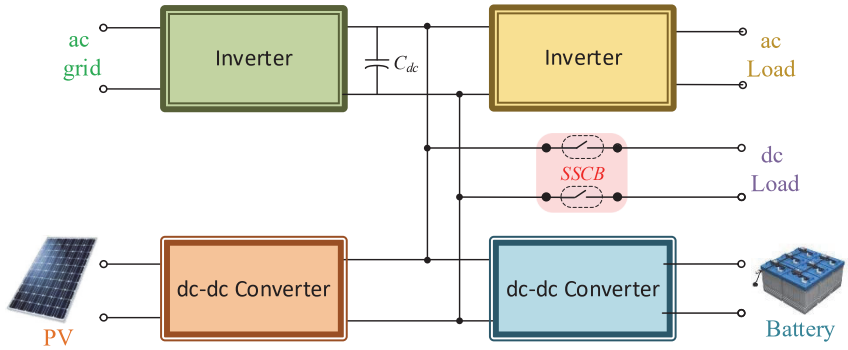


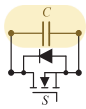
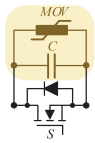
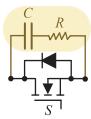
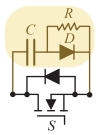
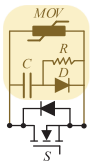
Figure 1. Structure of a typical energy router for residential application.

Direct current circuit breakers are mainly divided into three categories: electromechanical, hybrid, and solid-state circuit breakers. Electromechanical breakers typically cause arcs during the interruption and cannot meet the speed requirements for the protection of semiconductor-based converters. The arcs also erode the breaker contacts, which increases the maintenance costs [15]. To provide fast fault isolation without causing arcs, power electronic switches have been applied. A hybrid dc SSCB scheme, which is a combination of mechanical and solid-state technology, is now considered as an acceptable solution [16]. However, the mechanical ultrafast disconnector in these dc circuit breakers slows the current breaking process and increases their weight, volume, and investment price. With the development of electronic components, dc SSCBs have been greatly developed. They are extremely faster than mechanical and hybrid circuit breakers [17].

Solid-state circuit breakers are divided into two categories in terms of using either semi-controlled switching devices such as SCRs or fully controlled switching devices such as IGBTs and MOSFETS. Impedance-source SSCBs, which are the most popular solutions for using half-controlled switching devices, are reviewed in [18]. The SCR-based SSCBs benefit from smaller conduction losses, larger capacity, and lower price compared with the ones with fully controlled switches. However, since the turn-off process of SCR requires reverse voltage, the most important issue when designing an SCR-based SSCB is a reliable generation of a reverse voltage on the SCR during the turn-off process [19,20]. On the other hand, in SSCBs with fully controlled switching devices, there is full control of the breaking process.

When a short-circuit fault occurs in the system, a high di/dt is usually generated during the turn-off process of the SSCB, which generates serious dv/dt and overvoltage through the huge inductive energy applied across the main switches due to the transmission line inductance and current-limiting line inductors. It might exceed the device rating and cause failure [21]. Also, a high dv/dt can induce gate oscillation, gate-oxide degradation, and false turn-on, causing reliability and lifetime issues. To reduce this voltage, rise rate, and voltage spike, snubber circuits must be added. Various snubber configurations have been reported for SSCBs, which are reviewed in Table 1.

Table 1. Different types of snubbers including the pros and cons of each.

Snubber	Circuit	Pros and Cons
C		✓The snubber capacitor absorbs some of the energy stored in the inductance of the system by getting charged. This slows down the voltage rise rate and the peak voltage of the switching devices. ☒ When the switch is turning off, the capacitor oscillates with the inductance of the circuit. In addition, during the turn-on process, it causes a high discharge current through the switching device.
C + MOV		✓The varistor provides overvoltage protection using voltage clamping. ☒ When the switch is turning off, the capacitor oscillates with the inductance of the circuit. In addition, during the turn-on process, it causes a high discharge current through the switching device.
RC		✓The resistor damps the oscillations caused by the snubber capacitor and the system inductance being in series. It also decreases the turn-on current, which is discharged through power semiconductor. ☒ When the switch is turning off, the voltage drop across the snubber resistor is reflected on the switching device, which increases its peak turn-off voltage requirement of the switch.
RCD		✓This combination eliminates the additional drop of voltage across the resistor as well as significantly reduces the voltage oscillations during the turn-off. ☒ It includes more components.
RCD + MOV		✓In addition to the benefits of the RCD snubber, the varistor provides overvoltage protection using voltage clamping. ☒ It includes more components.

Reference [22] utilizes a metal-oxide varistor (MOV) with a capacitor to suppress the overvoltage during the turn-off process and analyzes the effects of capacitor variation on the voltage suppression capability. However, there are two major problems associated with a pure C snubber (even with a MOV), including the oscillation of the current because of the system inductance and the high discharge current during the turn-on process. By using a snubber resistor in series with the capacitor, the discharge current can be reduced and the current will be damped [23]. In addition, using a MOV in parallel with the RC snubber significantly reduces the required capacitance [24,25].

However, in an RC snubber (or RC + MOV), the voltage across the resistor is reflected on the power semiconductors during turn-off, which causes extra voltage stress and power shock [26]. Alternatively, a resistor-capacitor-diode (RCD) snubber can separate charging and discharging paths. The MOV-RCD snubber is analyzed in [27] using analytical investigations, where the short-circuit current capability, clearance time, and transient power shock are considered.

In this paper, a bidirectional SSCB is designed and prototyped, which isolates both the positive and negative terminals of the system quickly and efficiently. A complete set of formulas to calculate all time intervals, voltages, and currents is presented. In addition, a soft turn-on auxiliary is designed to prevent a high current surge caused by

the capacitance difference between the source and the load. The experimental results demonstrate the proper performance of the topology and the validity of the findings.

2. Investigation of the Topology

The topology is composed of two back-to-back MOSFETS, with an RCD snubber for each MOSFET as shown in Figure 2. On the negative side, there is a mechanical switch that gets turned off when the current of the circuit reaches almost zero. In traditional bidirectional SSCBs with two switches, just the positive terminal gets disconnected. Therefore, there will still be voltage on the components in the system. By using the mechanical switch, safety is increased and the disturbance in the system when using more than one SSCB gets suppressed [28]. This mechanical switch acts when the current of the circuit reaches very close to zero.

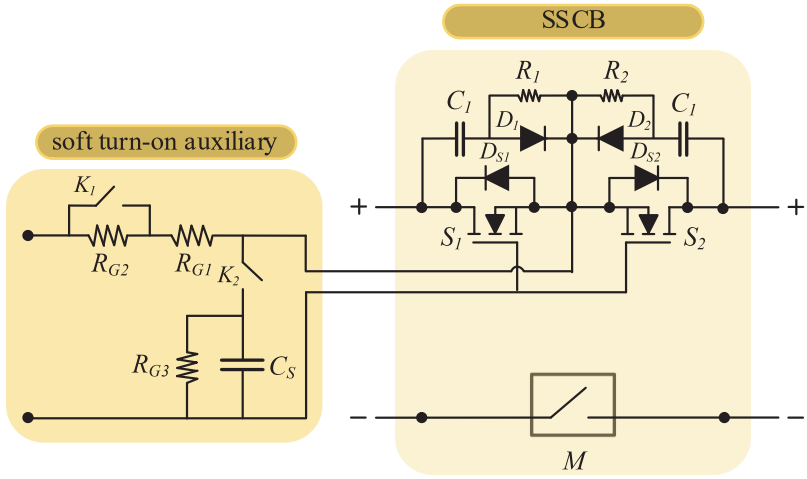


Figure 2. Designed dc SSCB with its soft turn-on auxiliary.

Figure 2 also represents an auxiliary circuit for the driver of the MOSFETs facilitating the turn-on process of the switches, which is crucial in the energy router applications that often face the voltage difference between the source and the load. This part is further discussed in Section 3.

The operating modes of the designed SSCB are shown in Figure 3. In the normal operation and even when the fault occurs before the reaction of the SSCB, the current flows through both MOSFETs (Figure 3a). When the short-circuit fault occurs, both MOSFETs get turned off but the current finds its way through the snubber capacitor and the snubber diode (Figure 3b). However, as the energy and current of the inductor reach zero, the current is reversed and flows through an RCL circuit, which prevents it from oscillating (Figure 3c). Finally, when the current of the circuit reaches zero, the mechanical switch M gets turned on and disconnects the dc source (Figure 3d).

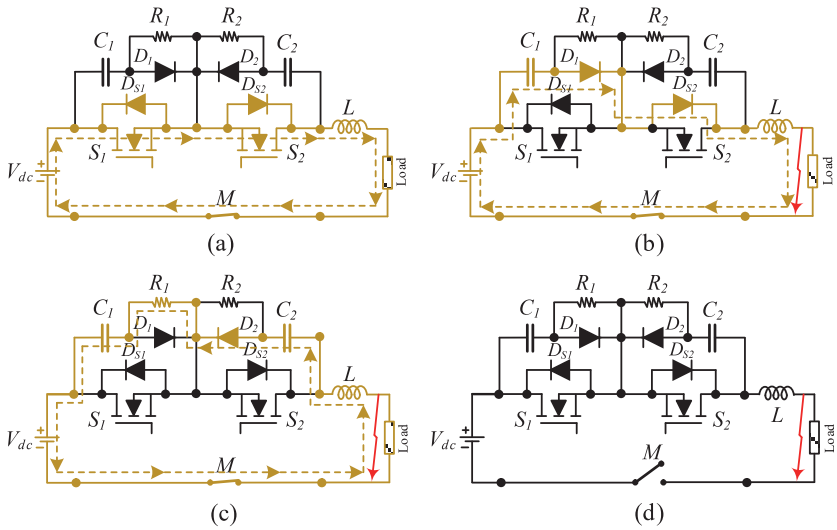


Figure 3. Operating modes of the SSCB. (**a**) stages 1 and 2, (**b**) stage 3, (**c**) stage 4, (**d**) stage 5.

2.1. Stage 1

The first stage is the normal mode when both switches are turned on, and the circuit breaker passes the current as shown in Figure 3a through the switches S_1, and S_2. As shown in Figure 4, it is evident that before t_1, the voltages of the capacitors and switches are zero and the current of the inductor is at its nominal value. For a simpler calculation, we assume $t_1 = 0$.

$$i_L = I_N \tag{1}$$

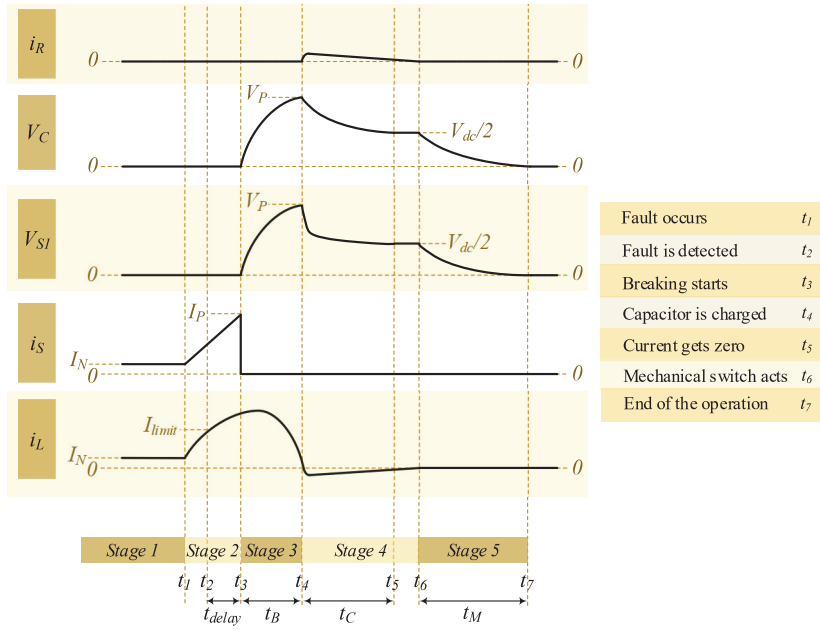


Figure 4. Operating waveforms of the SSCB.

2.2. Stage 2

In the $(t_1 - t_2)$ interval, at t_1 a short-circuit fault occurs at the output terminals and the current of the circuit increases to reach i_{limit} at t_2. i_{limit} is the current that is determined in the controller at which the SSCB should operate. By assuming $R_{SW} = R_{Line} = 0$, and initial value: $i_L(t = 0) = I_N$,

$$L\frac{di_L}{dt} - V_{dc} = 0 \tag{2}$$

By solving the above first-order differential equation, the current is calculated as follows:

$$i_L = \frac{V_{dc}t}{L} + I_N \tag{3}$$

By $i_L = I_{limit}$,

$$t_2 = \frac{L(I_{Limit} - I_N)}{V_{dc}} \tag{4}$$

However, t_2 is not the actual time that the SSCB acts since there is a delay in both the microcontroller and measurement system, which is named t_{Delay}. Therefore, the actual time of breaking is t_3.

$$t_3 = t_2 + t_{Delay} \tag{5}$$

By calculating t_{Delay} and consequently t_3 by (2), the maximum current of the switches is obtained as follows:

$$I_P = \frac{V_{dc}t_3}{L} + I_N \tag{6}$$

2.3. Stage 3

During the $(t_3 - t_4)$ interval, the current flows through the snubber *C* and the inductor of the line. Therefore, the following equations are derived:

$$L\frac{di_L}{dt} + V_C - V_{dc} = 0 \tag{7}$$

$$i_C = C\frac{dV_C}{dt} \tag{8}$$

$$i_C = i_L \tag{9}$$

The current of the inductor and the voltage of the capacitor can be obtained from the above equations by considering the initial values: $i_L(0) = I_P$ and $v_C(0) = 0$:

$$i_L = I_P \cos\frac{t}{\sqrt{LC}} + V_{dc}\sqrt{\frac{C}{L}}\sin\frac{t}{\sqrt{LC}} \tag{10}$$

$$v_C = V_{dc} - V_{dc}\cos\frac{t}{\sqrt{LC}} + I_P\sqrt{\frac{L}{C}}\sin\frac{t}{\sqrt{LC}} \tag{11}$$

t_B can be calculated by putting $i_L = 0$.

$$t_B = -\sqrt{LC}Arctang\left(\frac{I_P}{V_{dc}}\sqrt{\frac{L}{C}}\right) \tag{12}$$

The maximum voltage on the switches combined can be obtained by putting t_B in the equation of the capacitor voltage:

$$V_P = V_{dc} - V_{dc}\cos\frac{t_B}{\sqrt{LC}} + I_P\sqrt{\frac{L}{C}}\sin\frac{t_B}{\sqrt{LC}} \tag{13}$$

Therefore, the time that the voltage of the switch reaches its maximum is calculated as follows:

$$t_4 = t_B + t_3 \tag{14}$$

2.4. Stage 4

During the $(t_4 - t_5)$ interval, as the inductor's energy has reached zero, energy now flows from the charged capacitor to the inductor. However, because of the resistor in the path, the current of the circuit does not oscillate and reaches zero after t_C. Thus, the equation of the circuit in this stage is as follows:

$$L\frac{di_L}{dt} + V_C - V_{dc} + R_S i_L = 0 \tag{15}$$

$$i_C = C\frac{dV_C}{dt} \tag{16}$$

$$i_C = i_L \tag{17}$$

By solving the above second-order differential equation, the current is calculated as follows with the initial value: $i_L(0) = 0$, $v_C(0) = V_P$.

$$i_L = A_1 e^{S_1 t} + A_2 e^{S_2 t} \tag{18}$$

where:

$$S_1 = -\alpha + \sqrt{\alpha^2 - \omega^2}, S_2 = -\alpha - \sqrt{\alpha^2 - \omega^2}$$

$$\alpha = \frac{R}{2L},\ \omega = \frac{1}{\sqrt{LC}}$$

$$A_1 = S_1\Big(LC^2S_2 + L\Big)(V_P - V_{dc})\ ,\ A_2 = S_2\Big(LC^2S_1 + L\Big)(V_P - V_{dc})$$

Since the plot of i_L is exponential, the current of the inductor does not reach zero but it tends to zero, so by considering $i_L \leq \epsilon$, t_C will be obtained.

The time when the system is completely out of current is calculated as:

$$t_5 = t_C + t_4 \tag{19}$$

2.5. Stage 5

The system is out of current but there is still a dc input voltage connected. The mechanical switch starts to operate at the time $t_6 \geq t_5$ and the negative terminal of the circuit will be isolated. Finally, after t_M, the negative terminal is isolated, and the circuit is completely out of current and voltage at the time t_7.

3. Design Procedure

The design procedure of the SSCB is performed for both the circuit itself and its auxiliary circuit for the soft turn-on operation.

3.1. Short-Circuit Fault Operation

In order to find the optimized value of snubber capacitor C, the following assumptions can be considered to simplify the equations:

$$V_{dc} - V_{dc}\cos\frac{t_C}{\sqrt{LC}} \ll I_P\sqrt{\frac{L}{C}}\sin\frac{t_C}{\sqrt{LC}} \tag{20}$$

$$\sin\frac{t_C}{\sqrt{LC}} \approx \frac{t_C}{\sqrt{LC}} \tag{21}$$

Therefore, the peak voltage of the capacitor can be rewritten as follows:

$$V_P \approx I_P \frac{t_C}{C} \tag{22}$$

Therefore, the value of the capacitor is obtained using Equations (6) and (22):

$$C \approx \left(\frac{V_{dc} t_B}{L} + I_N\right)\left(\frac{t_C}{V_P}\right) \tag{23}$$

The minimum value of the snubber capacitor can now be obtained by considering V_{clamp} of the MOV as V_P. Therefore, based on the desired Δt_C, the optimized value of C can be found.

In order to obtain the optimal size of the snubber resistor, since the circuit forms an RLC circuit during stage 4, the formula of the inductor's current (Equation (18)) should be overdamped. In order to overdamp the current of the inductor, the following equation must be valid:

$$\alpha > \omega \tag{24}$$

where:

$$\alpha = \frac{R}{2L}\ ,\ \omega = \frac{1}{\sqrt{LC}}$$

Therefore, the minimum value of the snubber resistance is obtained as follows:

$$R > 2\sqrt{\frac{L}{C}} \tag{25}$$

3.2. Soft Turn-On Operation

When the fault is cleared and the system is going to run again, there is usually a voltage difference between the input and output voltage terminals, especially in the energy router applications in which the dc link is connected to some different energy sources. This voltage difference can create a huge current passing through the switches and running the SSCB. Therefore, the turn-on process should be as soft as possible.

The aforementioned problem is addressed using an auxiliary circuit for the switches. As shown in Figure 5a, it is assumed that there is a voltage difference between V_{dc} and V_O. If we consider the gate-source voltage of the MOSFET as shown in Figure 5b, for soft turn-on an RC circuit as demonstrated in Figure 5c is needed. Hence, the gate-source voltage (V_{GS}) can be calculated by solving the first-order equation of the RC circuit as follows:

$$V_{GS} = V_K\left(1 - e^{\frac{-t}{RC}}\right) \tag{26}$$

where V_K is the voltage of the gate driver. Time t can be considered as the minimum time needed for equalizing the voltages in the circuit. This depends on the capacitance of the input and output terminals and the resistance of the line.

$$t = 5RC \tag{27}$$

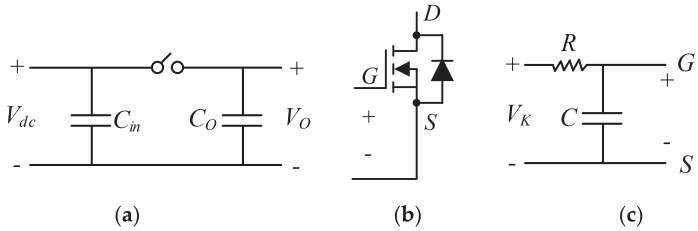


Figure 5. Circuits for calculation of the optimized values of R and C (**a**) The gate-source voltage of MOSFET, (**b**) the auxiliary circuit for the gate of the MOSFET, (**c**) The system with its capacitors of input and output.

The minimum gate-source voltage (V_{GS}) that can turn on the MOSFET can be obtained by testing a MOSFET or using the datasheet.

By placing V_{GS} and t in Equation (23), the value of RC can be calculated.

It now seems that the simplest solution for the soft turn-on is by placing a capacitor in parallel to the gate-source of the MOSFET and a resistor in series with the gate terminal. However, placing the capacitor will also affect the turn-off time. Thus, the solution is to increase the resistance R by placing a huge resistor in series with the gate terminal and turn-off resistor R_{G1}, and in parallel with a diode in the other structure so as not to affect the turn-off time (Figure 6a). In the other structure, the resistor and diode are placed in series together and in parallel with the turn-off resistor R_{G1} (Figure 6b).

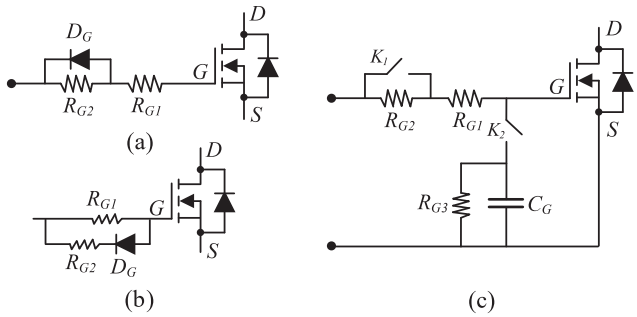


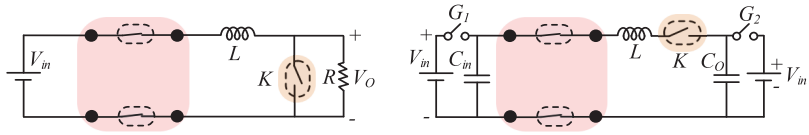
Figure 6. The MOSFET and its possible auxiliary circuits: (**a**) parallel approach, (**b**) series approach, (**c**) the main and complete approach.

However, the aforementioned solution severely affects the gate driver's performance. Therefore, the most complete approach is one using the structure in Figure 6c. In the turn-off mode, the mechanical relay K_1 is ON and relay K_2 is OFF. This means that only the resistor R_{G1} is in the gate auxiliary circuit. On the other hand, in the turn-on mode, the state of the relays K_1 and K_2 is reversed and they are turned OFF and ON, respectively, which puts the calculated RC in the gate auxiliary circuit. In this circuit, the resistor R_{G3} is in parallel with the capacitor to discharge the capacitor for the next turn-on.

4. Experimental Results

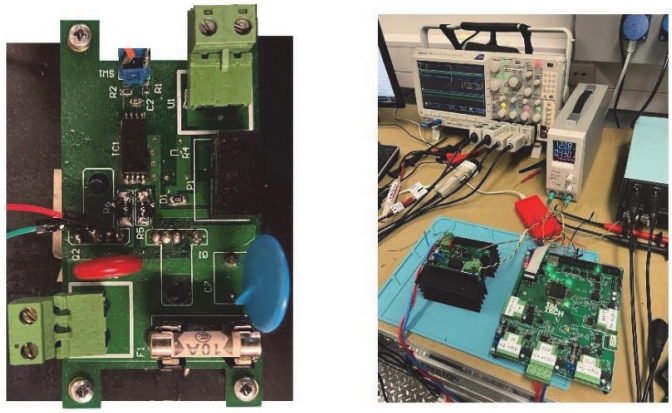
Figure 7 shows the schematic of the circuits used for the experiment. In the first experiment (Figure 7a), the short-circuit is created using a mechanical relay K across the load. Figure 8 shows the laboratory prototype and test operation of the designed SSCB. The design parameters of the designed SSCB are given in Table 2. In the first part of this test, the input voltage is 60 V and the limit current of the SSCB is 10 A. The result as shown in Figure 9a is a peak current of 44 A while the peak voltage of the switch S_1 is 270 V. In the second part of the test (Figure 9b), the voltage of the dc source is increased to 240 V

with a 30 A limit for the circuit's current. The SSCB breaks the circuit after 16 µs when the current reaches 100 A and the voltage of the switch S_1 reaches 420 V. As discussed before, in reality there is a time delay that depends on the current sensor and the speed of the microcontroller programming. The delay time of the current sensor used in this prototype is 14 µs and the delay of the programming equals the sampling period, which is 5 µs. These delays do not sum up since they occur simultaneously. This time delay can be reduced using a current sensor with a larger bandwidth.



(**a**) (**b**)

Figure 7. Test circuits. (**a**) Test circuit for short-circuit experiment. (**b**) Test circuit for soft turn-on experiment.

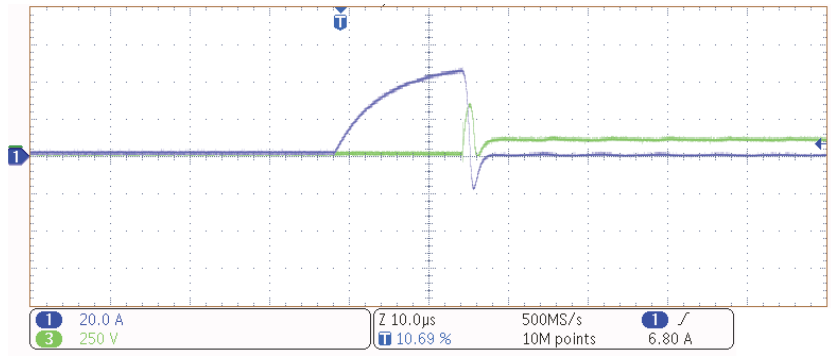


(**a**) (**b**)

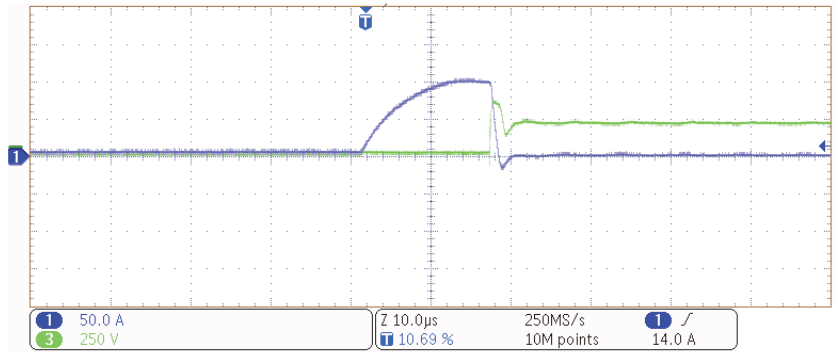
Figure 8. Laboratory prototype and test of the designed SSCB: (**a**) the prototype of the SSCB, (**b**) the test procedure of the SSCB.

Table 2. Design parameters of the designed SSCB.

Parameters	Acronym	Value	Unit
Input Voltage	V_{dc}	240	V
Snubber Capacitor	C_1& C_2	100	µF
Snubber Diode	D_1 & D_2	2	A
Snubber Resistance	R_1 & R_2	22	Ω
Line Inductor	L	10	µH
Clamp voltage of MOV	V_{Clamp}	675	V
MOSFETs		NTHL040N120SC1	
Capacitor of auxiliary circuit	C_G	100	nF
Resistance of auxiliary circuit	R_{G2}	10	kΩ



(**a**)



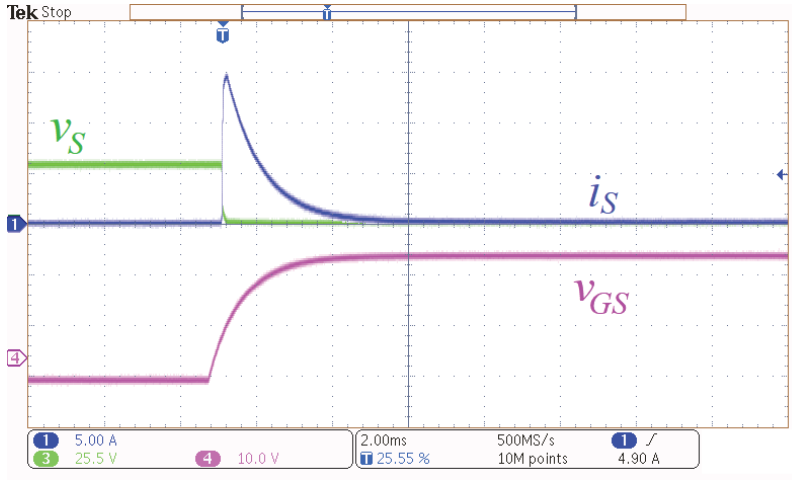
(**b**)

Figure 9. Experimental results of the short-circuit test: (**a**) V_{in} = 60, I_{limit} = 10; (**b**) V_{in} = 240, I_{limit} = 30.

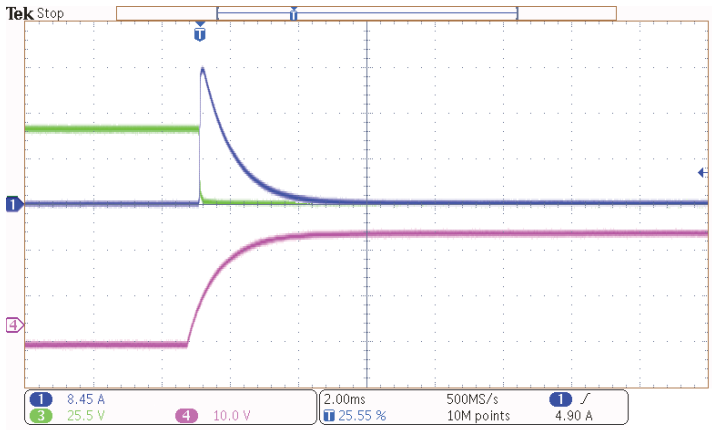
However, after reducing the time delay to the sampling period, to further decrease the delay, the sampling frequency should be increased. However, as discussed in the previous section this raises the peak voltage of the switch during the fault-clearing operation so there should be a lower limit for the delay according to the components' capability.

In the second test as shown in Figure 7b, the main path of the circuit is connected through a mechanical switch. The capacitors are then charged to different voltages by turning on the switches G_1 and G_2 temporarily. By disconnecting these switches and connecting switch K, there will now be a huge current spike because of the input and output capacitors' voltage difference dropped on the small resistance of the circuit. Therefore, the auxiliary circuit in Figure 6b is used in the main prototype for the soft turn-on.

As shown in Figure 10a, there is a 30 V voltage difference between the input and output capacitors, which by the benefit of using a 10 KΩ resistor and a 100 nF capacitor as mentioned before, the peak of the surge current is limited to 15 A. In the second test shown in Figure 10b, the voltage difference is 50 V, which is the maximum voltage difference in an energy router application. In this case, the peak surge current is 25 A, which is very desirable.



(**a**)



(**b**)

Figure 10. Experimental results of the soft turn-on test: (**a**) V_{dc} = 380, V_{out} = 350, (**b**) V_{dc} =401, V_{out} = 350.

5. Conclusions

An SSCB is designed for energy router applications with a soft turn-on capability. The findings of the working principles of the SSCB and its operating modes are used to propose an SSCB design procedure. An SSCB prototype is developed and its performance is evaluated in different operating scenarios for both short-circuit tests and soft turn-on tests. Although, using a relatively large resistor in series with the gate terminal and placing a diode in parallel with it to prevent its effect on the turn-off process reduces the turn-on surge current, it severely affects the gate driver's performance. Although, using a relatively large resistor in series with the gate terminal and placing a diode in parallel with it to prevent its effect on the turn-off process reduces the turn-on surge current, it severely affects the gate driver's performance. Therefore, by using two small low-voltage switches, an auxiliary circuit is obtained that solves the surge currents during the turn-on in the energy routers. The designed bidirectional SSCB uses an RCD+MOV snubber, which as discussed in the paper is the best snubber for circuit breakers switches. The SSCB breaks the circuit very fast at 16 µs. However, this time delay depends on the current sensor and the sampling frequency of the microcontroller programming. In this case, using a current sensor with a larger bandwidth can reduce the time delay to some extent, which should be

taken into consideration in the design procedure to find a balanced value as it increases the maximum voltage of the switches. On the other hand, the optimized value of the capacitor snubber is also calculated depending on the clamp voltage of the MOV and the desired time for discharging the line inductor's energy. This SSCB, unlike the traditional bidirectional SSCBs, benefits from isolating both terminals, which allows the circuit breaker to disconnect the voltage and the current, further increasing the safety and omitting the disturbance in the system when using more than one SSCB.

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Impedance-Source DC Solid-State Circuit Breakers: An Overview

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***Abstract*— Comparatively to an ac grid, it is easy to integrate distributed energy sources when implementing a dc microgrid. In addition, the efficiency and the reliability of the dc microgrid systems are higher than those of the ac system. However, the protection of the dc microgrid system including interruption and isolation of short-circuit fault currents remains an important concern. The traditional mechanical and hybrid circuit-breakers for dc fault protection have the drawback of slow operation, which requires a high rating power equipment. Solid-State Circuit Breaker (SSCB) is an optimal solution for fast dc fault interruption. Among different SSCBs, Impedance-Source Circuit Breakers (ISCBs) benefit from automatic fault detection and clearance because of using thyristors. In this paper, ISCBs are classified into five categories. These circuit breakers are reviewed by explaining the performance of each and mentioning some of their merits and drawbacks.**

Keywords—Circuit Breaker, Impedance-Source, Z-Source, Solid-State, T-Source, Γ-Source, Y-Source.

I. INTRODUCTION

Microgrids with dc power can offer higher reliability and power efficiency for many applications, including on-board DC power systems, in which distributed energy sources such as renewable energy sources and energy storage systems can be integrated seamlessly [1]. With a dc bus, problems such as harmonic, imbalance, and synchronization issues associated with ac systems are eliminated, leading to a greatly simplified control [2]. Furthermore, a higher power density is available because bulky traditional transformers used for ac–ac conversions are no longer required [3-5]. Consequently, the dc microgrid is becoming an attractive technology for on-board power systems [6].

However, as a critical technique to guarantee the safe operation of dc microgrids, dc circuit breakers are still a major technical obstacle to be surmounted due to the lack of a natural zero crossing in dc fault currents [7]. A dc circuit breaker (DCCB) is considered as a reliable method of isolating faults in dc systems quickly and selectively. However, since there is no zero crossing point in the current and also high fault current rising rate, the operation of interrupting the fault current in dc system is much more difficult compared with ac system. Therefore, the availability of DCCB becomes crucial, making it a key technology for dc system. Numerous DCCB topologies have been published and patented [2, 8].

DC circuit breakers are mainly divided into three categories: Electromechanical, hybrid and solid-state circuit breakers. Electromechanical breakers typically cause arcs during the interruption and cannot meet the speed requirements for the protection of semiconductor-based converters. Arcs also erode breaker contacts, which increases maintenance costs [9]. To provide fast fault isolation without causing arcs, power electronic switches have been applied. Hybrid DCCB scheme, which is the combination of mechanical and solid-state technology, is now considered as an acceptable solution [10]. However, the mechanical ultrafast disconnector in these dc circuit breakers, slows the current breaking process and increases their weight, volume, and investment price. With the development of electric power electronic components, dc solid-state circuit breakers have been greatly developed which are extremely faster than mechanical and hybrid circuit breakers [11].

An impedance-source network allows another state wherein the dc bus of the circuit can get short circuited during the normal operation [12]. Herein, this feature is adopted for fault handling in dc power systems. ISCBs are mainly composed of half-controlled device thyristors (SCRs). Compared with full-controlled switching devices such as IGBTs and MOSFETS, with much smaller conduction losses, larger capacity, and lower price is now gradually applied to design SSCB. However, since the turn-off process of SCR requires reverse voltage, the most important issue when designing an SCR-based SSCB (SCR-DCCB) is reliably to generate a reverse voltage on SCR during the turn-off process [13, 14].

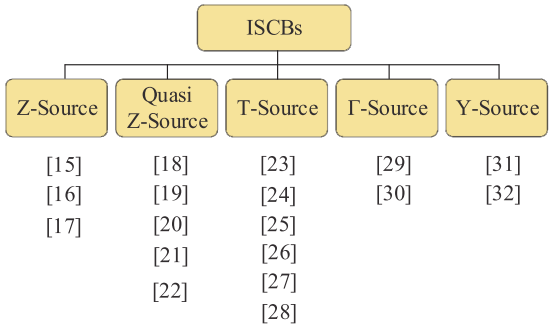

Fig. 1. The classification of ISCBs.

In this paper, various ISCBs are classified into six groups: Z-Source Circuit Breakers (ZCB), Quasi-Z-Source Circuit Breakers (QZCB), T-Source Circuit Breakers (TCB), Γ-Source Circuit Breakers (CB), and Y-Source Circuit Breakers (TCB). The working process of each circuit breaker is explained, and some advantages and disadvantage of some breakers is described.

II. ZSCBs

The earliest concept of the Z-source circuit breaker was proposed in [15] known as cross-connected ZSCB (Fig. 2(a)). When a fault occurs in the output terminal, a portion of the fault current will come from the ZSCB capacitances. In the transient state, the inductor keeps the current i_L constant. Current goes back to the source through capacitors. Which makes the capacitor current i_C increase until it reaches i_L. At this point, i_T will decrease to zero which causes the thyristor T_1 to commutate off. After that, the components of the z-source network are configured as two-series LC branches connected to the load and the fault. These circuits start a resonance where they are supplying the fault However, the output voltage decreases to zero because the source is disconnected, and the fault impedance is low. This topology has the advantage of fast reaction along with the fact that the fault current will not reflect to the source directly due to the presence of the inductor in the return path. However, it can be considered as a disadvantage since the source and the load do not have a common ground. In the working process of this cross-connected circuit breaker, a special mechanism must be attached to avoid the thyristor conducting again.

In grid applications with circuit breakers, some breakers are required to be closed quickly after staying open for a few microseconds. This causes disturbance in the system. Herein, another SCR facing the opposite direction can be added to the negative line of the breaker to create the circuit breaker in Fig. 2(b) which is proposed in [16]. In this topology, when a fault occurs, both positive and the negative terminal of the source get disconnected.

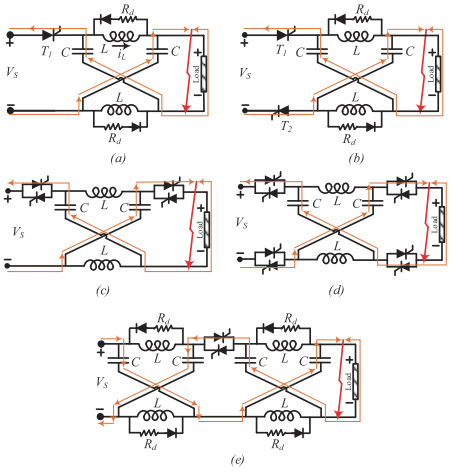

Fig. 2. The schematic of ZSCBs: (a) [15], (b) [16], (c) [16], (d) [17], (e) [17].

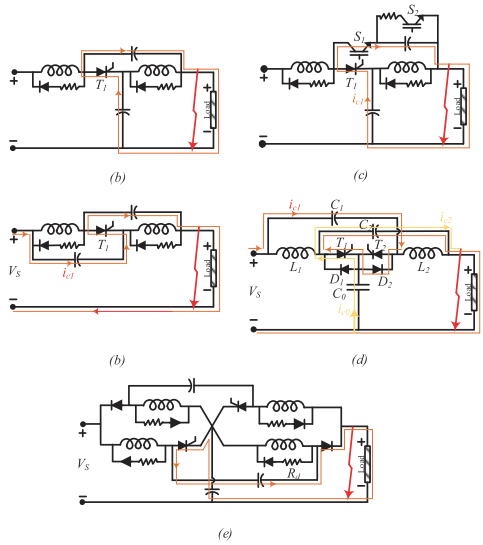

Fig. 3. The schematic of QZSCBs: (a) [18], (b) [19], (c) [20], (d) [21], (e) [22].

Figs. 2(c) and 2(e) show two possible ways to rearrange two ZSCBs to achieve the flexibility of bidirectional current flow [16, 17]. In both designs, it is possible to define the direction of the current flow by controlling the gate pulses of the thyristors. There are two advantages of using the design in Figure 2(e) which makes it the preferable option. Firstly, it has just one SCR in the path of conduction which means that it has half the conduction power losses compared to design in Figure 2(c). Secondly, the presence of an LC circuit before and after the SCR will add some delay in fault current propagation when a multiple of these breakers are connected in series. This delay time is useful in localizing the fault.

III. QZSCBs

The topology of the parallel-connected QZSCB is shown in Fig. 3(a) [18]. Compared with the cross-connected circuit breaker, it has two parallel LC branches, and it has a common ground between the load and the source. However, it can reflect a large current to the power source since there is no inductor in the return path and the high frequency conduction path through the capacitors of the Z-source is directly in-line with the source. During the steady-state operation, the load current flows through the z-source inductors. When a fault occurs, the current takes the high frequency path through the capacitors. As demonstrated in Fig. 3(a), this is in opposite direction with the current of the thyristor and results in commutation and the thyristor is naturally switches OFF.

The series connected circuit breaker which is proposed in [19], is shown in Fig. 3(b). When a fault happens, the transient fault current is supplied by both the Z-source capacitors and the load capacitor since the Z-source inductor current cannot change instantaneously. The Z-source capacitor current will increase until it reaches the Z-source inductor current. Then, the SCR experiences a current zero-crossing and is allowed to commutate off naturally. Once the SCR turns off, the two LC legs start a

resonance where they supply the fault from their respective energy storage. This resonance will continue until the inductor voltage tries to become negative. At this point, the snubber diodes turn on to steer the current away from the capacitors, and the current will continue to flow in the snubber loop until the energy stored in the inductor decays to zero. In comparison with ZSCBs, it has the advantages of having common ground and lower reflected current to the source. However, the current reflected to the source is still larger than that in the cross-connected circuit. Capacitor C_1 keeps charging during fault interruption and discharges through the thyristor during reclosure. This leads to high peak currents in the SCR.

As it was mentioned, the series connected circuit breaker has a large, reflected current to the source, which may damage semiconductor devices of the source converter. To reduce the reflected current, two power switches such as IGBTs are added as shown in Fig. 3(c) [20]. These IGBTs are operated in a mutually complimentary manner. During normal operation, S_1 is kept in ON state to provide a path for current in the event of fault. During this period S_2 is kept in the OFF state. When the dc system is not energized, S_2 is kept in ON state, such that the stored energy in capacitor C_1 is completely discharged and keep the capacitor ready for the next fault interruption.

Fig 3(d) demonstrates the intercross connected ZSCB proposed in [21]. In normal condition, the breaker connects the load to the power source through the inductors T_1 (or T_2) and D_1 (or D_2). In this condition, C_0 is charged to the source voltage and voltages of the other capacitors are zero. During initial moments after fault occurrence, the Z-source inductors keep the load current constant. So, fault impedance is supplied by both the load and Z-source capacitors. The high-frequency current passes through two routes which are depicted in Fig 3(d). The total transient currents of C_0 and C_1 are in reverse direction of the SCR current. This high-frequency current increases until reaches the SCR current. Then, the SCR current goes to zero and commutates off. After the SCR turns off, LC branches create a resonance circuit. This topology reduces the losses of the traditional ZSCBs to some extent. However, when T_1 or T_2 is turned off during the fault, the fault current will oscillate due to the freewheeling effect of the reverse parallel connection the diode D_1 or D_2, which is unfavorable for dc systems.

In the bidirectional QZCB proposed in [22], during the steady-state operation, the capacitor C_1 is charged to source voltage V_S. Conduction path is from source to load through T_1 and inductors. When a line-to-line fault occurs, the current through inductor remains nearly constant. The capacitor C_1 supplies fault current through T_1 and capacitor C_2 as highlighted in Fig. 3(e). Therefore, current flowing through T_1 immediately reduces to zero. During this transient period, voltage across T_1 is negative. Since gate pulse of T_1 is withdrawn, it naturally commutates. After T_1 turns off, Z-Source components are seen as series LC branch connected to source. Once capacitor C_2 is completely charged, it will block the flow of source current and hence source is completely isolated from system. At this point, freewheeling diodes become forward biased and current continues in the inductor-diode-resistor loop until inductor energy decays to zero.

IV. TSCBs

In ZSCBs, there is a risk of overcurrent in the source converter. To eliminate overcurrent, a TSCB is proposed in [23] In normal condition, the current flows from source to load through SCR and transformer. When a fault occurs as shown in Fig 4(a), the primary windings face opposite current which is coupled to the transient fault current through the secondary windings. If this current reaches the level of the normal current is, the SCR forward current forces commutations and the dc system is interrupted.

In the TSCB proposed in [24] which is demonstrated in Fig. 4(b), when a short circuit fault occurs, the T-source transformer is equivalent to self-coupling buck transformer and the mutual coupling generates reverse current to turn off the T_1, the reverse current reflected to the thyristor 1 side is the ratio of the T-source capacitance current to the transformer turns ratio.

For the circuit breaker proposed in [25], the current path during the fault is shown in Fig. 4(c). When a short-circuit fault occurs, the load voltage drops rapidly, and the fault current rises rapidly. The current of the coupled coil L_1 will be reflected by the coil L_2 to get a reverse current with the main circuit, which will make the current of the main circuit be quickly pulled to zero and turn off the T_1. When the fault current disappears, there is still energy left in the couple inductor. At this time, the coupled inductor will release its energy through the snubber circuits.

When a short-circuit fault occurs in the QZSCB proposed in [26], the fault current path is shown in Fig. 4(d). At this time, the capacitor will discharge instead of the power supply. A part of the current of the capacitor will flow through the coupled coil L_2 to maintain the fault current, and the other part will flow through the coupled coil L_1 to block the thyristor T_1.

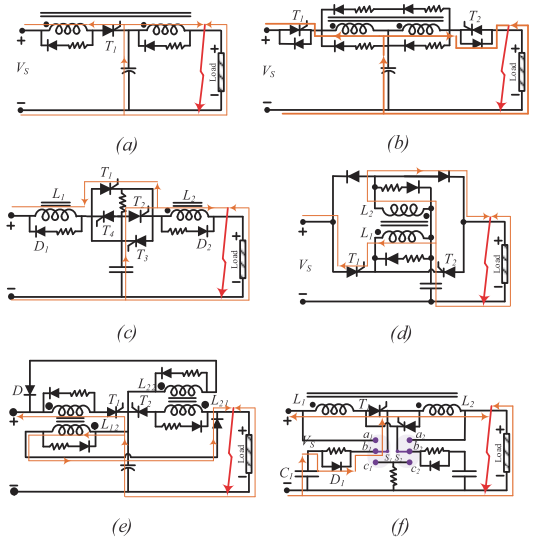

Fig. 4. The schematic of TSCBs: (a) [23], (b) [24], (c) [25], (d) [26], (e) [27], (f) [28].

In [27], under steady-state condition, a capacitor C is charged to the source voltage V_S. The current path is from source to the load through T_1 and coupled inductors L_{11} and L_{12}, as shown in Fig. 4(e). When a fault occurs as shown in Fig. 4(e), the capacitor starts discharging through L_{12} and D in the secondary branch. The magnetic flux in the core starts increasing. As a result, an induced voltage across L_{11} decreases the primary current and maintains constant magnetic flux in the core. With an increase in the current of L_{12}, the current of L_{11} starts decreasing. Hence, the resultant current through inductor L11 and T_1 reaches below holding current and it turns OFF. Once T_1 commutates, the fault is completely isolated from source and capacitor discharges through inductor L_{12}. At this point, free-wheeling diodes become forward biased and current continues to flow in the inductor–diode–resistor loop until the stored inductor energy decays to zero. Due to mutual inductance, there is no need of an additional Z-source capacitor as required in Bidirectional ZSCB to complete the fault current loop. Furthermore, the mutual inductance reduces the total inductance requirement, which in turn decreases the overall size, losses, and cost of the breaker.

In the converter proposed in [28], if the current flows from left to right, during the steady-state operation as shown in Fig. 4(h), the load current flows through the coupled inductor and T_1 to load resistance R_1. S_1 is switched at a_1 preparing for fault protection, and S_2 is switched at b_2 so that C_2 can maintain zero voltage in preparation for manual tripping. When a fault occurs, the primary will face a reverse current since it is coupled to the transient fault current through the secondary windings. It makes the SCR to commutate and turn off.

V. ΓSCBs

Flipped Γ-Source Circuit Breaker (FΓSCB) proposed in [29], benefits from relatively half elements in its structure in comparison with traditional ZSCBs. The operation principle of FΓSCB is similar to the previously discussed TSCB. When a short circuit fault occurs on the load side, as shown in Fig. 5(a), the capacitor discharges through the winding L_2 which makes an induced transient current in the winding L_1. Since this current is opposite to the forward current of the thyristor, it forces a current zero crossing in the thyristor to turn it OFF.

There is a slight difference in the working principle of the ΓSCB proposed in [30] where during the fault, as demonstrated in Fig. 5(b), the winding L_1 experiences a forward voltage and then induces a positive voltage across L_2. Since the capacitor is fully charged to the source voltage during normal operation, the L_2 voltage is reversely imposed on the thyristor which forces its current to zero instantly. Since the transient discharging current through L_2 must be considerably larger than the current of the winding L_1, the turns ratio of the transformer must be greater than 1. In the second step, as the current reaches zero, the SCR commutates off naturally and isolates the faulty section of the circuit from the source. Then, a resonance starts between the fault path and the Γ-source impedance network which continues until the voltage of inductor L_1 becomes negative. The snubber diode turns on in the third stage to consume the remaining energy in the damping resistor. A higher damping resistance can accelerate the energy dissipation; however, the voltage drop across the snubber is also increased, which means that an SCR with a higher voltage rating will be required.

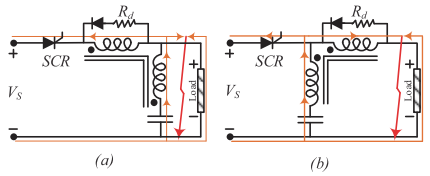

Fig. 5. The schematic of ΓSCBs: (a) [29], (b) [30].

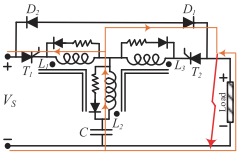

Fig. 6. The schematic of YSCB: [31], [32].

VI. YSCB

When the fault occurs in the YSCB proposed in [31], the capacitor C connected in series with the secondary coil L_2 is discharged and its current flows through the secondary coil of the transformer to compensate the fault current. Meanwhile, the primary coil L_1 makes the thyristor's current reach zero due to mutual inductance and the induced opposite current. Therefore, that the thyristor T_1 is turned OFF by the reverse voltage. As the thyristor is turned OFF, a resonant circuit is formed by the capacitor C and the secondary coil of the transformer L_2. The capacitor will generate a sinusoidal current: when the current direction is positive, the thyristor is turned OFF, and no current in the primary coil can be induced; when the current direction is negative, there will be induced current in the primary coil, and then consumed by the consumption circuit. When the capacitor is fully discharged, the current flowing through the inductor will reverse, and the excessive energy will be consumed by the RD snubber circuits [32].

VII. Conclusion

ISCBs are categorized into five classifications in terms of the impedance network used in them. ZSCBs and QZSCBs do not use coupled inductors which makes the design of their inductors easier in comparison with TSCBs, TSCBs, and YSCBs. However, they would need distinct magnetic cores which increases their volume. ZSCBs suffer from the amount of reflected fault current at the source which is an important factor to consider when designing and sizing the inductors and capacitors for ISCBs. Some QZSCBs has reduced or eliminated this factor. Common grounding is another feature that ZSCBs lack. Other ISCBs benefit from this feature. ISCBs in total, are much faster than traditional mechanical and hybrid circuit breaker, and more cost-effective because of using SCRs in comparison with other SSCBs. In addition, they do not need a detection system due to using SCR commutation to break the circuit automatically.

TABLE I. SUMMARY OF DIFFERENT ISCB TOPOLOGIES.

	Type	Num of Semiconductors	Num of Caps	Magnetic Components	Fault is Reflected to the source	Common ground	Bidirectional	RD Snubber	Ref
1	ZSCBs	1	2	2	Yes	No	No	2	[15]
2		2	2	2	Yes	No	No	2	[16]
3		4	2	2	Yes	No	Yes	-	[16]
4		8	2	2	Yes	No	Yes	-	[17]
5		2	4	4	Yes	No	Yes	4	[17]
6	QZSCBs	1	2	2	No	Yes	No	2	[18]
7		3	2	2	No	Yes	No	2	[19]
8		1	2	2	Yes	Yes	No	2	[20]
9		2	3	2	Yes	Yes	Yes	-	[21]
10		2	3	4	No	Yes	Yes	4	[22]
11	TSCBs	1	1	2	Yes	Yes	No	2	[23]
12		2	1	2	Yes	Yes	Yes	4	[24]
13		4	1	2	Yes	Yes	Yes	2	[25]
14		2	1	2	Yes	Yes	Yes	2	[26]
15		2	1	4	Yes	Yes	Yes	4	[27]
16		2	2	2	Yes	Yes	Yes	2	[28]
17	ΓSCBs	1	1	2	Yes	Yes	No	1	[29]
18		1	1	2	Yes	Yes	No	1	[30]
19	YSCB	2	1	3	Yes	Yes	Yes	3	[31, 32]

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[PAPER-VI] T. Hemmati Shahsavar, S. Rahimpour, N. Vosoughi Kurdkandi, A. Fesenko, O. Matiushkin, O. Husev, D. Vinnikov “Comparative Evaluation of Common-Ground Converters for Dual-Purpose Application,” Energies, vol. 16, no. 7, p. 2977, Mar. 2023.

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Comparative Evaluation of Common-Ground Converters for Dual-Purpose Application

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Abstract: The focus of this paper is to provide a comparative analysis of various common-ground converters that serve as dual-purpose power electronic interfaces. These interfaces are designed to be used in both DC and single-phase AC grids, utilizing the same terminals for both modes of operation. The idea lies in the utilization of the same semiconductors in the DC-DC and DC-AC configurations, resulting in minimal redundancy. Particular attention is focused on the comparative evaluation approach. A novel Flying Inductor (FI)-based converter was selected for experimental verification. The design example and experimental prototype of a dual-purpose DC-DC/AC power electronic converter is capable of providing 2 kVA of power in AC mode and 4 kW in DC mode. The experimental results indicate that the converter can operate in both AC and DC grids according to their respective modes. The conclusion of the study highlights the potential applications and main benefits of this technology.

Keywords: DC-DC power converter; DC-AC power converter; common-ground power converter; boost power converter; buck–boost power converter; leakage current

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1. Introduction

The ever-increasing energy needs of humanity are intensifying the exploration and development of new energy sources. Electrical energy consumption is expected to be doubled by 2050 [1]. Sustainable energies such as solar power, wind power, and other forms of Renewable Energy Sources (RESs) must contribute a noticeable percentage of electrical energy demand. Most RESs generate DC voltage. Among them, solar energy through Photovoltaic (PV) panels is one of the most important sustainable energy sources with DC nature. Power injection from RESs to the conventional AC grid is faced with certain problems. The concept of energy storage has become more important as a result of the increasing penetration of RESs. They can balance the grid. Energy storage is mostly carried out with DC voltage. A rechargeable battery is the main storage form. The DC form of RESs and the storage batteries revive the topic of DC microgrids [2,3] and make them a modern trend [4–6]. They do not have conventional issues of the AC grid such as harmonics, reactive power control, frequency stability, etc. Taking into account both technical and economic factors, the most suitable DC voltage level appears to be 326 V [7]. However, other research indicates that a voltage level between 350 V and 380 V could become a standard in the future [8]. A three-wire DC grid configuration is proposed, consisting of +350 V, −350 V, and a neutral point. Additionally, a 700 V DC grid is being considered as a microgrid for integrating renewable energy sources (RESs). While DC grids have advantages in terms of efficient energy transfer, they may not be compatible

with most household devices as most infrastructure is based on alternating current (AC). Therefore, it can be concluded that implementing DC technology rapidly is limited by the need for AC-based power electronics infrastructure.

The lack of a viable business model is another hurdle that must be overcome in order to implement a DC grid. Power electronics manufacturers are hesitant to produce DC appliances and promote the growth of the DC market, while investors are not yet convinced of the potential demand for DC technology. This uncertainty about the DC market is discouraging large market players from investing in DC solutions.

In light of the advantages of DC technology and the challenges associated with its implementation, it is believed that power electronic converters capable of functioning in both DC and AC applications could be a promising solution. The dual-purpose DC-DC/AC approach offers a means to minimize investment risks in DC infrastructure and provide greater flexibility for consumers. This concept is illustrated in Figure 1 and has been explored in several sources, including [9–12].

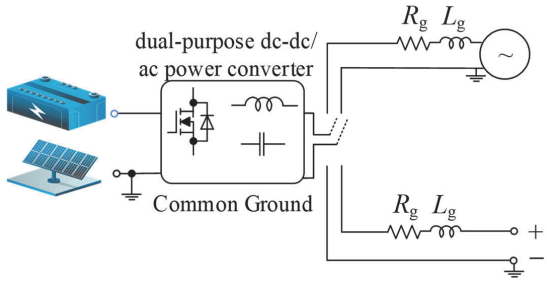


Figure 1. Dual-purpose DC-DC/AC power converter with common-ground architecture concept.

Design, implementation, and efficient operation of DC infrastructures are topics of discussion. They should be considered in dual-purpose DC-DC/AC power converters as well. One of the key issues to be taken into consideration is protection [13], and corrosion is one of its important aspects. It results from the electro-chemical process in a concrete structure such as a building. Concrete contains salt. The DC leakage current is conducted by metal and makes it anodic. The reaction between the anodic metal and the existing salt leads to the production of oxygen which makes the environment corrosive. Therefore, the metal slowly corrodes and dissolves the reinforcement. One solution to tackle leakage current is an earth leakage circuit breaker. This can switch off the installation if the leakage current reaches a certain value. In other words, if the leakage current stays below the specified value, the circuit breaker does not operate, and the metal reinforcement is in danger. Even several milliamperes of DC leakage current can create a corrosive environment. The damage of a DC leakage current is 100 times higher than the damage of an AC leakage current of the same size. Hence, using an earth leakage current circuit breaker is not an appropriate idea. Corrosion problems can be solved if leakage currents are prevented from flowing through the earthing facilities. In order to achieve this goal, sources are earthed indirectly through a capacitor diode network. The diodes block the leakage currents as long as the applied voltage remains below the diode voltage. The number of capacitor diode networks depends on the number of decentralized sources. In the case of several decentralized sources, a single ground point is not sufficient. This affects the system grounding configuration, and consequently a greater number of capacitor diode networks is required. Moreover, this solution is suitable for DC power systems. If the dual-purpose DC-DC/AC power converter operates in an AC power grid, another approach is required to suppress AC leakage. This burdens the system.

In most cases, there are numerous methods available for designing the grounding system in an electrical power network, and each of these approaches can lead to varying levels of performance outcomes [14]. It is important to note that the primary purposes of grounding are for identifying ground faults and ensuring the safety of personnel and

equipment [15]. Low-Voltage (LV) DC microgrids can be grounded through high resistance or low resistance. The ground can be connected either to one of the poles or to the middle point if it is available. Low-resistance grounding means that the grounded wire has a very similar potential to AC grids. The opposite case in DC systems requires only high-resistance grounding and cannot eliminate leakage current, which in turn leads to corrosion problems.

The way of grounding depends on the interconnection between AC and DC grids. Figure 2 shows different scenarios of DC grids where the grounding can be realized by low impedance on both sides. First of all, power flow between AC and DC microgrids can be provided by low-frequency transformers and non-isolated front-end rectifiers (Figure 2a). Figure 2b shows an isolated ac-DC converter. Finally, Figure 2c shows a non-isolated power electronics interface. The last solution does not have any redundancy. Moreover, it requires DC-AC energy conversion with common ground. The used transformers in the first two solutions impose a high volume to the system and decrease its efficiency. The common-ground architecture is a suitable approach for DC and AC systems in terms of full elimination of the DC and AC leakage currents. It could be a suitable candidate for dual-purpose DC-DC/AC power converters. Furthermore, such types of converter can be used as interfaces between DC and AC grids.

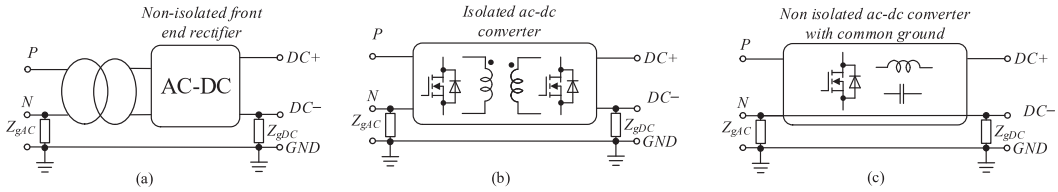


Figure 2. Schematics of existing solutions for power flow between AC and DC microgrids: (**a**) non-isolated front-end rectifier, (**b**) isolated ac-DC converter, and (**c**) non-isolated power converters with common-ground architecture.

There are many DC-AC converters with common-ground architecture [16–24]. They also have the capability of dual-purpose DC-DC/AC operation. The Switched-Capacitor (SC) or Flying Capacitor (FC) solutions [16,17] and their derivatives [18] have common-ground features. However, they cannot realize a boost mode and suffer from inrush current.

Multilevel SC-based structures are presented in [19–24]. These structures can also inject power to the grid at an input voltage lower than the peak grid voltage; however, their main shortcoming is inrush currents. Moreover, their voltage-boosting factor is constant.

Meantime, several novel common-ground solutions suitable for dual-purpose application have been already presented [25–27].

The main goal of this work is to provide comparative analysis of common-ground solutions suitable for dual-purpose DC-DC/AC applications. Prior to previously presented dual-purpose solutions, the novel common-ground Flying Inductor (FI) DC-AC converter [28] is selected for design and experimental verification for dual-purpose application. The selected DC-DC/AC power converter is evaluated and compared with existing dual-purpose DC-DC/AC power converters.

The paper is organized as follows. Section 2 is devoted to the comparison between existing solutions. Section 3 describes the operation principle of the selected FI solution. Section 4 is devoted to the components' design guidelines example. Section 5 is devoted to the prototype description and experimental verification. Finally, the main design challenges and conclusions are presented and discussed in Sections 6 and 7, respectively.

2. Comparison Study

In this section, the aim is to compare dual-purpose DC-DC/AC power converters with common-ground features.

Figure 3 shows the circuit of an FI DC-AC converter presented in [28], as one of the novel family of FI inverters. By means of this example, we demonstrate that many solutions

with additional suppressor capacitor C_S and Solid-State Circuit Breakers (SSCB) for very fast disconnection in case of any emergency can be used for dual-purpose applications. It was shown in [9].

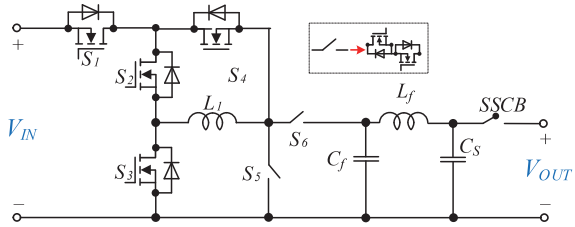


Figure 3. FI-based universal DC-DC/AC interface converter [28].

To compare different solutions for dual-purpose DC-DC/AC power conversion, the unfolding circuit with a buck–boost converter from [9] is used as a reference solution. Other options that are specifically designed for this purpose include the FC power converter in [25] and the FI-based power converter in [27]. In addition, many of the latest inverters and multilevel inverters are capable of operating in both DC-DC and DC-AC modes. For the purposes of comparison, the five-level SC-based inverter from [24] and the FI-based power converter from [29] are also evaluated. The schematics of these solutions are shown in Figure 4. All of the solutions are common ground, except for the buck–boost converter and the unfolding circuit from [9]. While the unfolding circuit can significantly reduce leakage current, it cannot eliminate it entirely.

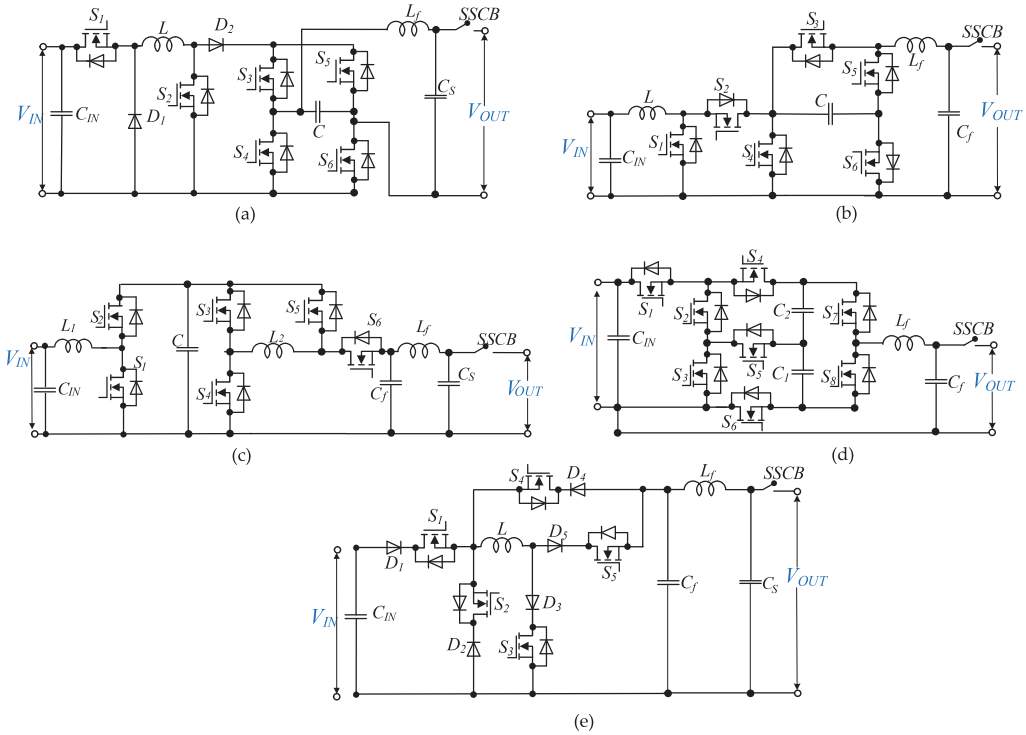


Figure 4. Schematics of the compared topologies: (**a**) buck–boost and the unfolding circuit in [9], (**b**) FC power converter in [25], (**c**) FI power converter in [27], (**d**) SC power converter in [24], and (**e**) FI power converter in [29].

In [25], a dual-purpose power converter is introduced. It is based on the FC circuit and operates as a three-level inverter. During DC-DC and DC-AC conversion, a capacitor is used to pump energy into the negative output voltage. On the other hand, the inverter in [24] is based on the SC circuit and uses two capacitors as voltage sources in the negative half cycle. Although the virtual voltage source concept is used in [24,25], they differ in terms of capacitor charging. In [25], the capacitor charges smoothly through a charging inductor, while in [24], the capacitors charge directly from the voltage source at the switching frequency, resulting in current spikes. In contrast, the unfolding circuit in [9] uses a virtual capacitor that functions as a current source.

Similar to the selected dual-purpose FI power converter, the introduced power converters in [27,29] are based on FI circuits, and the required energy is pumped from the inductors to the output. Among the compared topologies, the SC power converter in [24] has a fixed double-voltage boosting capability, while other solutions can operate under a wide range of input voltages.

It is aimed to discuss the advantages and disadvantages of each structure. To reach this goal, it is important to pay attention to the point that each structure is designed, built, and tested under different conditions; hence, it is not possible to make a fair comparison. However, the fundamental waveforms of a typical converter are independent of the component type and electric parameters (e.g., switching frequency and selected semiconductors). To put it differently, the primary wave forms are produced through the fundamental modulation method, which establishes certain overall requirements for component sizing. These requirements involve estimating passive component values, which can be achieved by considering equal current ripples in the inductors and identical voltage ripples across the capacitors.

In (1) and (2) the maximum accumulated energy inside a capacitor and an inductor are calculated, respectively. According to these equations, the volume of a core of an inductor as well as the volume of a capacitor can be estimated:

$$Vol_C \cong W_C = \sum_{i=1}^{N_C} C_i.\hat{v}_{Ci}^2 \tag{1}$$

$$Vol_L \cong W_L = \sum_{i=1}^{N_L} L_i.\hat{i}_{Li}^2 \tag{2}$$

In (1), C_i and N_C are the capacitance of the ith capacitor and the number of capacitors, respectively. Furthermore, $\hat{v}_{Ci}$ represents the peak voltage of the ith capacitor. In (2), L_i and N_L are the inductance of the ith inductor and the number of inductors, respectively. In addition, $\hat{i}_{Li}$ is the peak inductor current.

The losses of conductivity in relation to the switch current are directly proportional to the square of the current, and are independent of semiconductors. Total conduction losses can be obtained by (3):

$$P_{CON} \cong \sum_{i=1}^{N_S} \tilde{i}_{Si}^2 \tag{3}$$

Finally, we can estimate the Total Standing Voltage (TSV) across the semiconductors:

$$TSV \cong \sum_{i=1}^{N_S} \hat{V}_{Si} \tag{4}$$

Based on the above-mentioned points, we provided the same condition for all the selected topologies in the PSIM environment under equal conditions as the following.

The inductors were selected to have a current ripple equal to 20% of their current ratings. With this assumption, the used charging inductor in [9,25] is 3.3 mH, the two inductors in the flying inductor power converter in [27] are 1 mH, the inductor in the flying

inductor power converter in [29] is 1.1 mH, and the inductor in the selected dual-purpose DC-DC/AC power converter is 1 mH.

The capacitors were selected to have a voltage ripple equal to 10% of their voltage ratings. With this assumption, the used capacitor is 10 uF in the FC-based power converter in [25], is 2 uF in the buck–boost and unfolding circuit in [9], is 300 uF in the FI-based power converter in [27], and is 1600 uF for C_1 and 680 uF for C_2 in the SC-based inverter in [24].

The output filter for the selected dual-purpose DC-DC/AC power converter, the FI-based power converter in [27], the FI-based power converter in [29], and the buck–boost and unfolding circuit in [9] is a CL type. The output filter for the FC-based power converter in [25] and the switched-capacitor inverter in [24] is a CL type. In all the compared topologies, the output filter capacitor is 3.3 uH. It should be noted that the used capacitor in the unfolding circuit acts as the output filter capacitor and is equal to 2 uF. There is no additional output filter capacitor in this topology. In the selected topology, the inductance of the output filter inductor is 500 uH. It results in 2.53% Total Harmonic Distortion (THD) in the output current. Hence, the output filter inductors are selected to have the same THD in the output current. Based on this assumption, the output filter inductor is 750 uH for the buck–boost and unfolding circuit in [9], is 1700 uH for the FC-based power converter in [25], is 1 uH for the FI-based power converter in [27], is 700 uH for the FI-based power converter in [29], and is 2000 uH for the SC-based power converter in [24].

The parameters in Table 1 were considered for all the compared topologies to simulate the same conditions.

Table 1. Simulation parameters.

Parameters	Values
input voltage (V_{IN})	200 V
peak value of the output voltage (V_{out})	325 V
switching frequency (fs)	25 kHz
average output power (P_{out})	1 kW

The power switches in the circuit were assumed to have an on-state resistance of 0.028 Ω, which is the internal resistance of the NVHL020N120SC1 switch, a type of N-channel MOSFET power switch with a body diode. In contrast, the power switches used in a previous power converter design (referenced as [29]) were Insulated Gate Bipolar Transistor (IGBT) power switches without body diodes, which limit the current to flow in only one direction. MOSFETs, on the other hand, have bidirectional current flow capability inherently. To account for the unidirectional current flow in the IGBT-based design, a diode was added in series with the power switch in the simulation. For power diodes, the on-state resistance ($R_{on,D}$) was assumed to be 0.05 Ω, and the forward voltage ($V_{fw,D}$) was assumed to be 0.65 V in the circuit models.

The comparison between different circuit designs focused on several key factors, including the accumulated energy of capacitors (W_C), the accumulated energy of inductors (W_L), the Total Standing Voltage (TSV) of the semiconductors, conduction losses of the semiconductors (P_{CON}), and the number of power switches used (N_{SW}). It has been previously discussed in reference [25] that a smaller number of power switches does not necessarily result in higher efficiency, and this issue will also be explored in the current discussion.

Figure 5 presents a radar chart comparing the different circuit topologies based on their calculated parameters shown in per unit values. The inverter introduced in reference [24] uses an SC circuit and has the highest capacitor value among the compared designs, resulting in high accumulated energy in the capacitors. However, this topology also has significant conduction losses. Switched-capacitor circuits are susceptible to current spikes that occur when the capacitors are being charged, causing inrush currents to pass through the power switches in the charging path, leading to higher current stress and power losses. As the output power increases, the magnitude of these current spikes becomes higher,

potentially damaging the power switches. Therefore, SC-based solutions are not suitable for high-power applications. The FI power converter in [29] has the highest value of conduction losses due to power losses across the series-connected power diodes with the power switches. In contrast, the selected dual-purpose DC-DC/AC power converter, the FC-based power converter in [25], and the buck–boost unfolding circuit in [9] have the lowest accumulated energy in the capacitors. The selected dual-purpose DC-DC/AC power converter and the introduced power converter in [29] use FI architecture, and the filter capacitor is the only capacitor used in their configuration. The dual-purpose converters in [9,25] use a pseudo DC-link approach, which significantly reduces the capacitor size while maintaining good grid current quality. In terms of accumulated energy inside the inductors, the selected dual-purpose power converter stands out among the compared topologies, while the FI-based power converter introduced in [29] ranks highest. Regarding TSV, the introduced flying inductor dual-purpose converter in [27] has the highest voltage stress across its power switches.

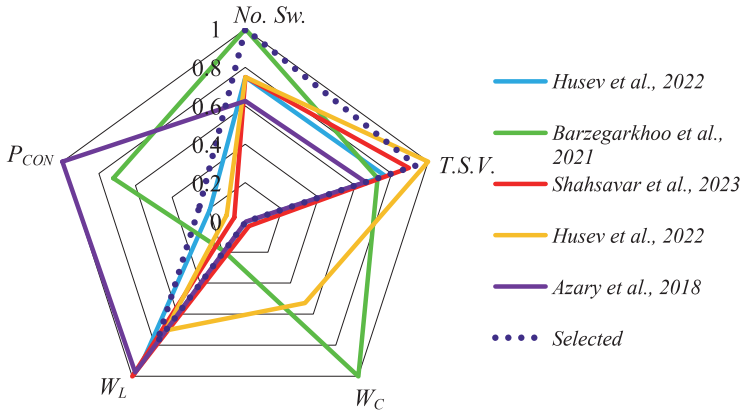


Figure 5. Radar chart of the compared topologies in [9,24,25,27,29].

3. Introduction to the Selected Solution Based on an FI Circuit

The topology selected for this study, as depicted in Figure 3, is based on a Flying Inductor (FI) circuit. The FI circuit operates by receiving and storing electrical energy from the input source at one point in time and delivering it to the output at another point in time, in a periodic switching cycle. One significant advantage of this topology is that it eliminates leakage current completely, by directly connecting the negative polarities of the input voltage source and the output side. This enhances the quality of power injected into the AC grid and improves system efficiency. To handle the bidirectional voltage stress on switches S_5 and S_6, a back-to-back combination of MOSFET switches is employed. Additionally, to minimize conduction losses on the input side, switch S_1 is utilized instead of a diode and functions as an active diode. In comparison to a previously introduced FI-based topology [30], the selected converter's inductor current is bidirectional under a DC-AC operating mode. Moreover, the converter's buck–boost capability enables power injection into the output grid over a broad range of DC input voltages.

The bi-directional nature of the selected dual-purpose DC-DC/AC power converter is especially valuable for energy storage systems that rely on batteries. It is particularly useful for home-scale storage systems that can charge batteries during low-consumption periods of the grid and discharge the stored energy into the grid during peak consumption periods using the selected dual-purpose DC-DC/AC power converter. The operation of the selected converter is examined below in both DC-AC and DC-DC modes.

3.1. Buck–Boost Operation Mode

In more technical terms, the selected dual-purpose DC-DC/AC power converter is capable of operating in two modes: buck–boost and buck. The buck–boost mode, which is characterized by symmetrical operation states, allows the converter to operate independently of the input voltage. This mode involves the storage of energy in the FI L_1 during one time period, followed by the injection of this energy into the output filter and the grid during another time period. This cycle repeats periodically, ensuring a continuous flow of power.

Positive output voltage generation:

When the output voltage is positive, the selected dual-purpose DC-DC/AC power converter operates in two equivalent circuits, as shown in Figure 6a,b. In the first circuit, switches S_1, S_2, and S_5 are turned on to allow current to flow through the input source and charge inductor L_1, while the other switches are turned off. The output filter L_f's current flows through capacitor C_f, creating a free-wheeling mode in the positive half cycle. The bi-directional SSCB switch remains operational in all modes, disconnecting the converter from the grid side in case of system errors to prevent voltage spikes. In the second circuit, switches S_3 and S_6 are turned on to transfer the stored energy in inductor L_1 to the output filter and the grid, while other switches are off.

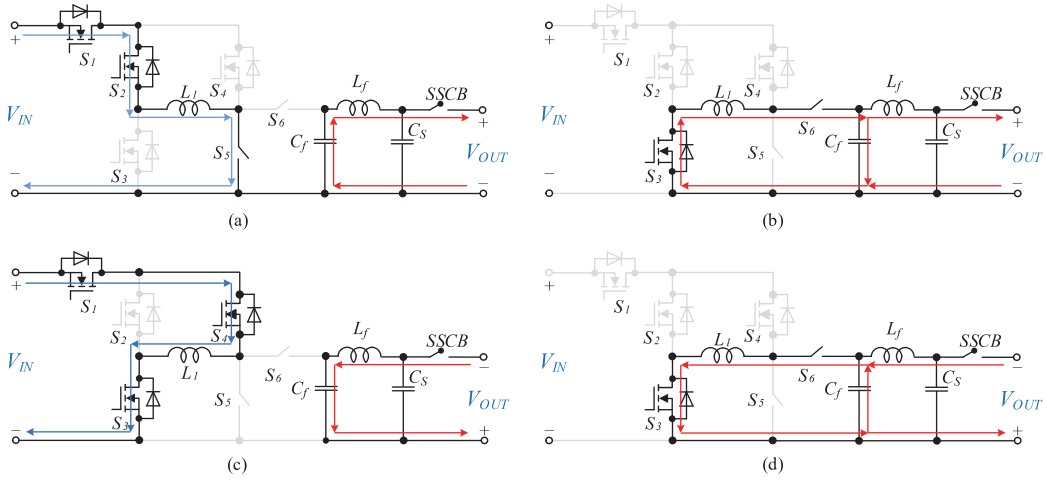


Figure 6. Equivalent circuits of the selected topology in the buck–boost (symmetrical) mode: (**a**) first equivalent circuit during positive output voltage generation, (**b**) second equivalent circuit during positive output voltage generation, (**c**) first equivalent circuit during negative output voltage generation, and (**d**) second equivalent circuit during negative output voltage generation.

Negative output voltage generation:

To generate a negative output voltage, the buck–boost mode is employed in the selected power converter. In this mode, the direction of the current in inductor L_1 is opposite to that of the positive output voltage generation. Switches S_1, S_3, and S_4 are turned on, providing a charge path for L_1. The current of the output filter L_f flows through the capacitor C_f. The equivalent circuit for this mode is depicted in Figure 6c.

The second equivalent circuit in case of negative output voltage generation is shown in Figure 6d. It can be called the active mode when switches S_3 and S_6 are turned on, and the stored energy in inductor L_1 is pumped to the output.

In the selected converter, the currents of switches S_3 and S_6 are bidirectional, while the current of other switches is unidirectional. Furthermore, the charging path of inductor

L_1 is shown by a blue line in operating modes and the output current path is shown by a red line.

3.2. Buck Operation Mode

The selected converter has flexibility in the case of positive output voltage generation. It depends on the value of input voltage. If the input voltage is less than the output voltage, the operating modes of the converter will still be the same as in the buck–boost mode, which is that described in Figure 6a,b. However, when the value of the input voltage is greater than the instantaneous value of the output voltage, then the converter will operate in the buck mode. The first equivalent circuit of the buck mode is shown in Figure 7a. In this mode, unlike in the buck–boost state, the inductor L_1 is used as a filter. This causes the current of inductor L_1 to be less in the positive output voltage generation than in the negative half cycle. In this case, switches S_1, S_2, and S_6 are conducting, and S_4 and S_5 are completely off. The second equivalent circuit of the second operating mode is shown in Figure 7b. In this case, switch S_2 turns off and switch S_3 turns on. In other words, switch S_3 acts as a freewheeling switch. Furthermore, in this mode, although the current of switch S_1 is zero, the pulse of this switch is still established. If the input DC voltage is higher than the peak value of output voltage, then only the buck mode can be utilized.

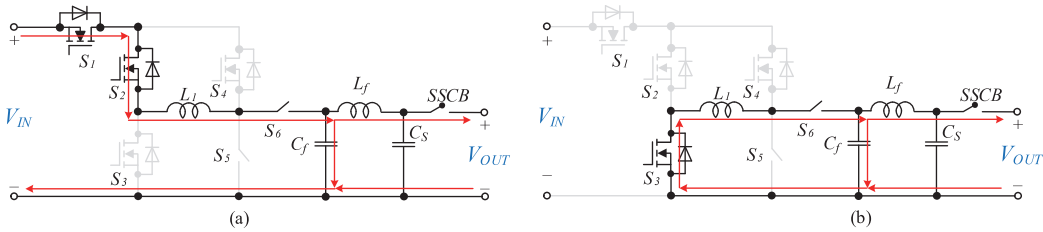


Figure 7. Equivalent circuits of the selected topology in the buck (asymmetrical) mode: (**a**) first operation mode—positive half cycle, and (**b**) second operation mode—positive half cycle.

From that written above, it is possible to conclude that in the DC-AC mode, the converter can be operated in both buck–boost and buck modes, which depend on the value of the input voltage. In the DC-DC mode, if a positive voltage is required at the output terminals, the operating modes will be the same as in Figure 6a,b. Furthermore, if a negative voltage is required at the output, then the operating modes of the selected converter will be the same as in Figure 6c,d. Since the negative terminals at the input and output are interconnected, it is best to use a positive polarity in the DC-DC mode as in Figure 6a,b. Due to the symmetrical shape of the inductor current, the buck–boost mode can be called a symmetrical mode, while the combination of buck and buck–boost can be called asymmetrical.

4. Passive and Active Component Design Guidelines

In this section, the values of active and passive elements are designed. The used switches are selected based on the rate of voltage and current stress. In addition, the value of passive elements is calculated based on the amount of output power.

4.1. Design of the Flying Inductor L_1

In this section, the value of the FI L_1 is designed. The volt-second balance rule is applied for inductor L_1 to calculate the inverter switching duty cycles as follows:

$$d(t) = \frac{v_{Cf}}{v_{Cf} + V_{IN}} \tag{5}$$

In (5), V_{IN} and V_{cf} refer to the input voltage, and the voltage across output filter capacitor is C_f. The output filter inductor has a smaller value; hence, the voltage drop across this inductor is small at the grid frequency, causing the capacitor voltage C_f (V_{Cf}) to be almost equal to the output voltage. The output voltage is also expressed as follows:

$$v_{out}(t) = V_{o,\max} \sin \omega t \tag{6}$$

In the above relation, $V_{o,\max}$ is the peak output voltage. By considering the equality of the output voltage and V_{cf}, and substituting (6) into (5), the inverter switching duty cycle is expressed as follows under the buck–boost mode:

$$d(t) = \frac{V_{o,\max} \sin \omega\, t}{V_{o,\max} \sin \omega\, t + V_{IN}} \tag{7}$$

The charging and discharging time of inductor L_1, defined by T_{on} and T_{off}, is calculated as follows:

$$T_{on} = \frac{d(t)}{f_S} = \frac{V_{o,\max} \sin \omega\, t}{f_S \cdot (V_{o,\max} \sin \omega\, t + V_{IN})} \tag{8}$$

$$T_{off} = 1 - \frac{V_{o,\max} \sin \omega\, t}{f_S \cdot (V_{o,\max} \sin \omega\, t + V_{IN})} \tag{9}$$

Here, f_S and T_S are the switching frequency and switching time period of the inverter, respectively. The current ripple of inductor L_1 is expressed as follows:

$$\Delta I_{L1} = \frac{1}{L_1} \int_0^{dT_S} v_{L1} dt \tag{10}$$

Taking $d(t)$ from (7) and substituting it into (10), the inductance value of L_1 is obtained as follows:

$$L_1 = \frac{V_{o,\max} V_{IN} \sin \omega\, t}{\Delta I_{L1} \cdot f_S (V_{o,\max} \sin \omega\, t + V_{IN})} \tag{11}$$

Given that the maximum ripple current of inductor L_1 occurs at the peak voltage of the grid, the value of the inductor L_1 is expressed as follows based on the maximum ripple current:

$$L_1 = \frac{V_{o,\max} V_{IN}}{\Delta I_{L1,\max} \cdot f_S (\, V_{o,\max} + V_{IN})} \tag{12}$$

The value of inductor L_1 in (12) is rewritten in (13) according to the average value of output power P_{out}, the average input voltage, the peak of output voltage, and the switching frequency, as follows:

$$L_1 = \frac{{V^2}_{o,\max} \cdot {V^2}_{IN}}{f_S \cdot P_{out} \cdot (\, V_{o,\max} + V_{IN})^2} \tag{13}$$

4.2. Design of the Output Filter Inductor and Capacitor

The equation of the output load current or AC grid current in the unity power factor is expressed by the following relation:

$$i_{out}(t) = I_{o,\max} \sin \omega t \tag{14}$$

During T_{on}, inductor L_1 is charged from the input source and the current of the filter L_f passes through capacitor C_f. Therefore, the voltage ripple of this capacitor is expressed as follows:

$$\Delta V_{Cf} = \frac{1}{C_f} \int_0^{T_{on}} I_{o,\max} \sin(\omega t)\, dt = \frac{I_{g,\max}}{C_f \cdot \omega} (1 - \cos(\omega T_{on})) \tag{15}$$

$$\Delta V_{Cf} = \frac{I_{g,\max}}{C_f \cdot \omega} (1 - \cos(\omega T_{on})) \tag{16}$$

By applying relation (8) to (16) and simplifying it, the capacitance of capacitor C_f can be calculated as follows:

$$C_f = \frac{2P_{out}}{(2\pi f_g)\Delta V_{Cf} \cdot V_{o,\max}} \left(1 - \cos\left(\frac{2\pi f_g \cdot V_{o,\max} \sin \omega t}{f_S \cdot (V_{o,\max} \sin \omega t + V_{IN})}\right)\right) \tag{17}$$

Since the maximum voltage ripple of capacitor C_f occurs at the peak voltage of output, the capacity of this capacitor can be calculated based on the maximum voltage ripple, as follows:

$$C_f = \frac{2P_{out}}{(2\pi f_g)\Delta V_{Cf} \cdot V_{o,\max}} \left(1 - \cos\left(\frac{2\sqrt{2}\pi f_g V_{rms}}{f_S \cdot \left(\sqrt{2}V_{rms} + V_{IN}\right)}\right)\right) \tag{18}$$

The value of the L_f filter inductor can be obtained based on the cut-off frequency of the output filter. For this purpose, the following relationship is established:

$$L_f = \frac{1}{C_f(2\pi f_C)^2} \tag{19}$$

In the above, f_c is the corner frequency of the output filter.

4.3. Current and Voltage Stress of the Selected Topology

In the selected converter, at time T_{on}, inductor L_1 is charged from the input source and delivers its energy to the output at the T_{off} interval. A part of the switches charges this inductor from the input source and another part discharges it by transferring energy to the output. Therefore, in this topology, all switches have the same current stress equal to the current passing through inductor L_1. The current equation of inductor L_1 based on the output current and the value of the switching duty cycle is expressed as follows:

$$i_{L_1}(t) = \frac{1}{1 - d(t)} \cdot i_o(t) + \frac{\Delta i_{L_1}(t)}{2} \tag{20}$$

The maximum duty cycle occurs at the peak output voltage and is expressed as follows:

$$D_{\max} = \frac{V_{o,\max}}{V_{o,\max} + V_{IN}} \tag{21}$$

Therefore, the peak current of inductor L_1 is determined based on the peak value of output current, maximum ripple current, and maximum duty cycle, as follows:

$$I_{L_1,peak} = \frac{2(V_{IN} + V_{o,\max}) \cdot P_{out}}{V_{IN} \cdot V_{o,\max}} + \frac{V_{o,\max} V_{IN}}{2L_1 \cdot f_S(\ V_{o,\max} + V_{IN})}. \tag{22}$$

$$I_{L1,peak} = \frac{4L_1 f_S (V_{IN} + V_{o,\max})^2 \cdot P_{out} + V^2{}_{o,\max} V^2{}_{IN}}{2L_1 \cdot f_S \cdot V_{IN} \cdot V_{o,\max}(\ V_{o,\max} + V_{IN})} \tag{23}$$

The stress of all switches is equal to Equation (24). The voltage stress of the switches varies. For example, as long as the input voltage is less than the peak value of output voltage, then the voltage stress of switch S_1 is as follows:

$$V_{S_1} = V_{o,\max} - V_{IN} \tag{24}$$

In addition, if the input voltage is higher than the peak value of output voltage, then the internal diode of switch S_1 is always conducting and the voltage of this switch is zero. The voltage stress of other switches is also given below:

$$V_{S_2} = V_{S_5} = V_{o,\max} \tag{25}$$

$$V_{S3} = V_{IN} \tag{26}$$

$$V_{S_4} = V_{S_6} = V_{IN} + V_{o,\max} \tag{27}$$

5. Experimental Verification

In this section, a number of experimental results of the selected converter are presented in order to evaluate its performance. The active and passive device components used in the practical results section are shown in Table 2.

Table 2. Passive elements and components used in the experimental results.

Element	Type	Description
Power switches	NVHL020N120SC1	1200 V/103 A
FI L_1	Ferrite core	407 uH
Output filter L_f	Iron powder	100 uH
Input voltage	DC	100–400
Output voltage	DC/AC	350 V/230 V rms
Output filter C_f	Film capacitor	3.3 uF/400 V
Microcontroller	Texas Instrument	TMS320F28379D
Switching frequency	-	25 kHz

The value of inductor L_1 is also obtained from Equations (12) and (13) by considering the appropriate current ripple. The TMS320F28379D microcontroller is specifically designed for power electronic applications and features 24 Pulse Width Modulation (PWM) channels and four Analogue to Digital Converters (ADCs) with the ability to handle up to 12 external channels. Its primary function in this context is to control switches and SSCB relay and generate PWM pulses. If the selected topology's requirements in terms of PWM and ADC channels can be met by a less expensive microcontroller, it can be substituted. The control system used for this converter is a Model Predictive Control (MPC) that has been investigated in a previous study (reference [31]). The input voltage source is a PV simulator type, which allows testing of the converter under real conditions when connected to a solar panel system. Experimental results have been obtained for both DC-AC and DC-DC modes. A laboratory prototype of the selected converter is shown in Figure 8. The converter has buck–boost capability, enabling it to operate over a wide range of input voltages, typically ranging from 100 to 400 V. In DC-AC mode, the output voltage is 230 V RMS, while in DC-DC mode, it is 350 V.

When operating in the buck or asymmetric mode, as shown in Figure 7, the current of inductor L_1 is smaller than in the symmetric or buck–boost mode when the output power is held constant. This is primarily due to direct energy transmission from the input source to the output, with inductor L_1 acting as a filter. In the symmetric or buck–boost mode, energy is first stored in inductor L_1 and then delivered to the output, resulting in a higher inductor L_1 current. As a result, the system efficiency is better in the asymmetric mode than in the symmetric mode, and the experimental results are therefore discussed more in the context of an asymmetric mode.

5.1. DC-AC Mode

The objective in the DC-AC mode is to produce a sinusoidal AC voltage at the converter's output terminals, regardless of a wide range of variations in the input DC voltage. Figure 9a depicts the input current (I_{dc}), FI current (I_{L_1}), input voltage (V_{dc}), and output voltage (V_{OUT}) from top to bottom. The figure shows that the input voltage is 200 V DC, while the output voltage is 230 V RMS, with an output power of 1.5 kW.

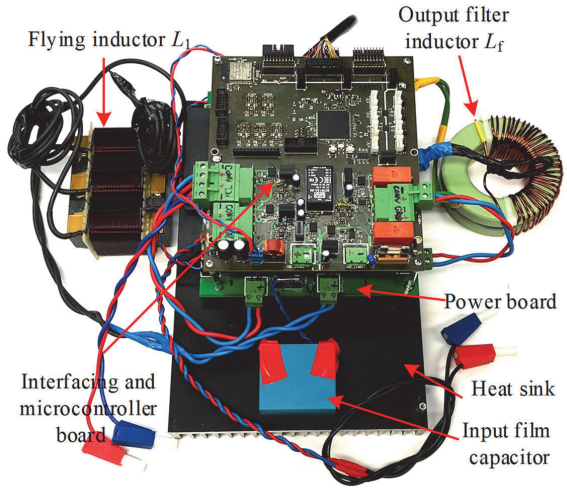


Figure 8. Control and power boards of the selected topology's laboratory prototype.

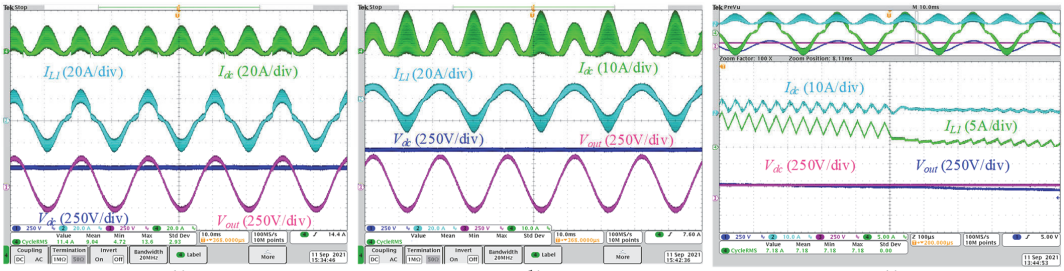


Figure 9. Experimental results in asymmetrical operation mode: I_{dc}, I_{L_1}, V_{dc}, and V_{OUT} from top to bottom, respectively; (**a**) at the input voltage of 200 V and output power of 1.5 kW, (**b**) at the input voltage of 400 V and output power of 2 kW, and (**c**) zoom mode of I_{dc} and FI current at V_{dc} of 150 V and output power of 1 kW.

As shown in this figure, the dual-purpose DC-DC/AC power converter operates in buck mode when the output voltage's instantaneous value is less than the input voltage value, and it switches to buck–boost mode when the output voltage's instantaneous value is greater than the input voltage value. From Figure 9a, it is evident that the current of inductor L_1 is not symmetrical in the positive and negative half cycles. However, despite this asymmetry in the inductor current, the output voltage remains symmetrical.

Figure 9b displays I_{dc}, I_{L_1}, V_{dc}, and V_{OUT} per 2 kW output power. In this figure, the converter's applied voltage is 400 V. As the input voltage is higher than the output voltage's peak value, the dual-purpose DC-DC/AC power converter operates in buck mode during the positive half cycle and buck–boost mode during the negative half cycle. Inductor L_1 acts as a filter during the positive half cycle, causing the current in this interval to be lower than that in the negative half cycle. Figure 9b also demonstrates that the input current in the positive half cycle is lower than that in the negative half cycle. Nevertheless, despite the asymmetric performance of the converter, the output voltage remains perfectly symmetrical. The converter's efficiency can be enhanced by reducing the current in the positive half cycle or making the converter operate asymmetrically.

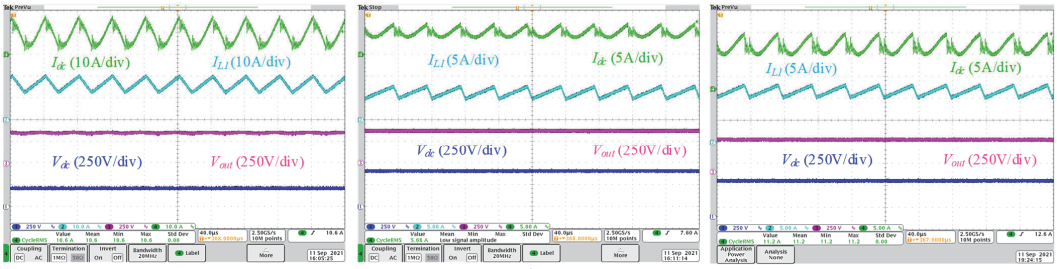
Figure 9c illustrates I_{dc} and I_{L_1} at the moment when the converter changes from buck–boost to buck mode. As indicated by the figure, the input current ripple and inductor current L_1 are lower in buck mode than in buck–boost mode. Moreover, the converter's

operation switches without a transient state, as demonstrated in the figure. Despite this change, the output voltage remains sinusoidal.

5.2. DC-DC Mode

This section discusses the experimental results of the selected converter in the DC-DC operation mode. The selected converter has a buck–boost capability, which enables it to operate over a wide range of input voltages. The objective is to generate a 350 V output DC voltage while varying the input voltage between 200 V and 400 V. The converter can produce both positive and negative polarity voltage at the output, but generating positive polarity voltage is preferred as the converter can also operate in the buck mode, leading to improved efficiency. Moreover, generating positive polarity voltage creates a common connection between the input and output terminals.

The information presented in Figure 10a illustrates the input current (I_{dc}), FI current (I_{L_1}), output voltage (V_{OUT}), and the input voltage (V_{dc}), from top to bottom. The input voltage depicted in this figure is 200 V, whereas the output voltage is 350 V, indicating that the power converter selected for this demonstration is in buck–boost mode with a duty cycle exceeding 0.5, as discernible from the waveform of inductor L_1 current. Moreover, this figure shows that the output power is 2 kW. Figure 10b shows I_{dc}, I_{L_1}, V_{OUT}, and V_{dc} from top to bottom, respectively. In this figure, the input voltage is equal to 400 V and the output voltage is 350 V in its previous value. In addition, the output power is 2 kW. Due to the fact that in this figure the input voltage is more than the output voltage, the selected dual-purpose DC-DC/AC power converter operates under the buck mode. In this case, the duty cycle needs to be around 0.875. The L_1 inductor current ripple verifies this issue. The performance of the selected converter at higher power is demonstrated in Figure 10c. At this level, the output power is approximately 4 kW, and the input voltage is 400 V. Similar to Figure 10b, the converter functions in buck mode in Figure 10c due to the output voltage being lower than the input voltage.



(a) (b) (c)

Figure 10. Experimental results in DC-DC operation modes: I_{dc}, I_{L_1}, V_{OUT}, and V_{dc} from top to bottom, respectively; (**a**) at the input voltage of 200 V and output voltage of 350 V and 2 kW, (**b**) at the input voltage of 400 V and the output voltage of 350 V and 2 kW, and (**c**) at the input voltage of 400 V and output voltage of 350 V and 4 kW.

Based on the information presented in Figure 10, it can be inferred that the selected dual-purpose DC-DC/AC power converter has the capability to generate a constant DC voltage on the output terminal, even with a variable input voltage. This converter topology can be employed in DC grids. The selected converter utilizes two four-quadrant switches, and precise adjustment of the dead time is necessary in these switches. For instance, during the positive half cycle, the dead time must be accurately set between switches S_5 and S_6, and during the negative half cycle, it should be precisely adjusted between switches S_4 and S_6. Failure to fine-tune the dead time between the switches can result in increased losses and voltage spikes in the switches.

Figure 11a,b depicts the voltage stress on switch S_4, current stress of inductor L_1, and voltage stress on switches S_5 and S_6, respectively, from top to bottom. In Figure 11a,

the dead time between the switches is appropriately adjusted, resulting in an acceptable voltage spike across the switches. Lower voltage spikes across the switches aid in reducing switching losses. In contrast, in Figure 11b, the dead time between the switches is not correctly adjusted. This leads to an increased voltage spike in the switches, resulting in higher switching losses. Additionally, an incorrect dead-time setting between the switches may cause the switches to malfunction, owing to the high voltage spikes. Figure 11c demonstrates the performance of the chosen converter during output power step changes. In this instance, the input voltage is 400 V, and the converter is in buck–boost or symmetrical operation mode. The output power has risen from 1 kW to 2 kW with the increase in load, doubling the input and inductor L_1 current values. From Figure 11c, it is evident that the output voltage remains stable at the time of output load step changes, indicating that the converter can handle these conditions effectively.

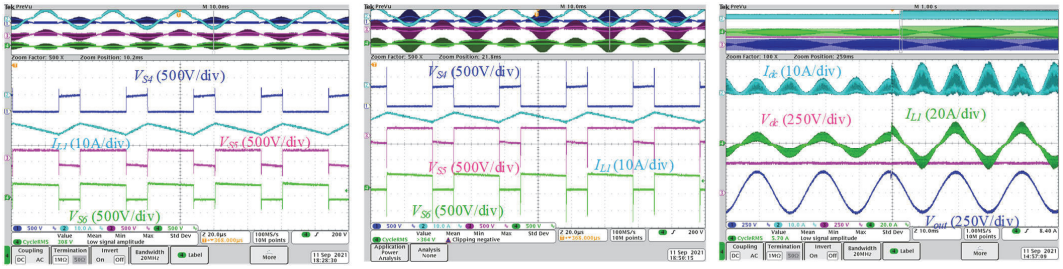


Figure 11. Experimental results of voltage stresses of the switches: voltage stress of switch S_4, FI current, voltage stress of switch S_5, and voltage stress of switch S_6 from top to bottom, respectively; (**a**) with precise adjustment of dead time between the switches, (**b**) without precise adjustment of dead time between the switches, and (**c**) the input current, FI current, input voltage, and output voltage at the step change of output power from 1 kW to 2 kW and with input voltage of 400 V.

Figure 12 is presented to demonstrate the performance of the chosen dual-purpose DC-DC/AC power converter under step-change conditions. The aim is to produce a step change in the peak output voltage, while the input voltage remains constant at 200 V. In Figure 12a, a step change is implemented in the reference value of the output voltage, with the intention of increasing the peak output voltage from 220 V to 325 V. As depicted in the figure, the output voltage follows the step change, and the output voltage of the selected converter remains stable. Furthermore, the output power increases from 0.5 kW to 1 kW in this figure. In Figure 12b, unlike Figure 12a, the objective is to decrease the peak value of the output voltage. In this figure, a step change is implemented at the output voltage, resulting in a reduction of the peak value of the output voltage from 325 V to 220 V. Additionally, the output power decreased from 1 kW to 0.5 kW. Figure 12c depicts I_{L_1}, output current (I_{OUT}), V_{dc}, and V_{OUT} from top to bottom, respectively. The input voltage is 400 V, and the output power is 1.5 kW. This figure is presented to illustrate the operation of the chosen converter in transient mode, from symmetric to asymmetric modes and vice versa. The symmetric and asymmetric operating modes are determined based on the flying inductor current value. As demonstrated in the figure, the output voltage remains constant in both symmetric and asymmetric operating modes. In other words, the control system maintains the output voltage at its nominal value.

The purpose of Figure 13a,b is to demonstrate the capability of the selected converter to control reactive power. This figure displays I_{L_1}, V_{dc}, V_{OUT}, and I_{OUT} when operating at leading and lagging power factors. It can be concluded from the figure that the dual-purpose DC-DC/AC power converter can effectively function at power factors other than unity. Figure 13c illustrates the voltage stress experienced by switches S_1 to S_3 in the converter. The input voltage is set at 200 V in this figure. It can be observed that the correct

dead time between the switches has been set, as the spike voltage of the switches appears to be within normal range.

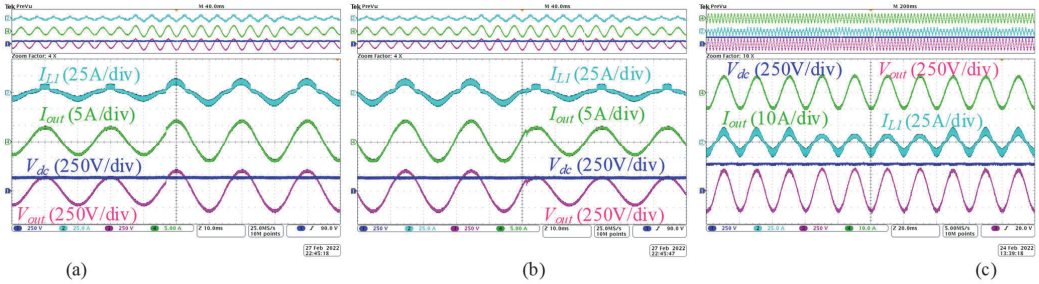


Figure 12. Experimental results in transient conditions: I_{L_1}, I_{out}, V_{dc}, and V_{OUT} from top to bottom at the input voltage of 200 V; (**a**) step change in peak value of output voltage from 220 V to 325 V and output power change from 0.5 kW to 1 kW, (**b**) step change in peak value of output voltage from 325 V to 220 V and output power change from 1 kW to 0.5 kW, and (**c**) I_{out}, I_{L_1}, V_{dc}, and V_{OUT} from top to bottom with the input voltage of 400 V and output power of 1.5 kW in the transient condition from symmetric to asymmetric operation mode and vice versa.

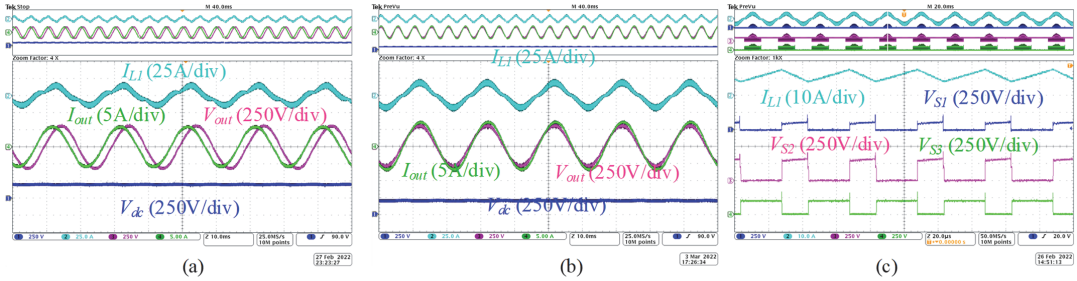


Figure 13. Experimental results in reactive power modes: I_{L_1}, V_{OUT}, I_{OUT}, and V_{dc} from top to bottom at input voltage of 200 V and output apparent power of 1 kVA; (**a**) with power factor of 0.7 leading, (**b**) with power factor of 0.96 lagging, and (**c**) voltage stress of the switches S_1, S_2, and S_3.

Figure 14a shows the input current, flying inductor current, input voltage, and output voltage from top to bottom, respectively. The purpose of this figure is to show the input voltage changes and to keep the output voltage constant for these changes. In Figure 14a, the converter's input voltage is raised from 200 V to 400 V. The output voltage remains constant despite the increase in input voltage. This figure portrays how the control system operates when the input voltage changes while maintaining a constant output voltage. Additionally, the output power is maintained at 1 kW, which leads to a decrease in both the input current and flying inductor current as the input voltage increases. Figure 14b demonstrates that even when the input voltage is lowered from 400 V to 200 V, the control system maintains a constant output voltage. Moreover, since the output power is held constant at 1 kW in this figure, the reduction in input voltage causes an increase in both the input current and the flying inductor current. Figure 14c displays the output current, flying inductor current, input voltage, and output voltage in response to changes in output power. In this figure, the input voltage is 400 V, and the output power is increased from 1 kW to 2 kW. The figure indicates that increasing the output power from 1 kW to 2 kW results in an increase in both the output current and flying inductor current, while keeping the output voltage constant at its previous value.

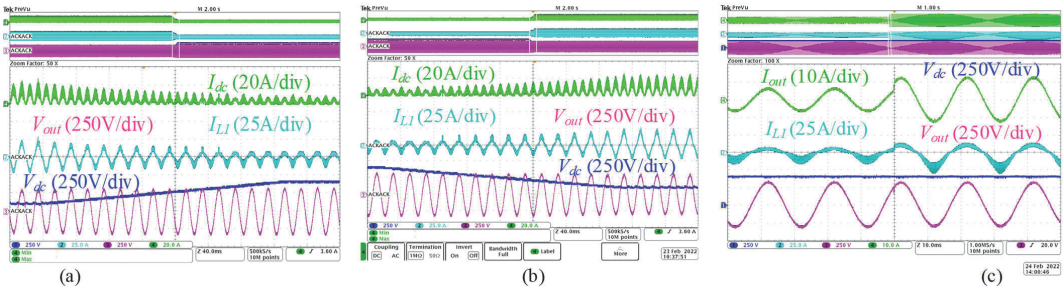


Figure 14. Experimental results in transient states: I_{dc}, I_{L_1}, V_{dc}, and V_{OUT} at output power of 1 kW; (**a**) changing in input voltage from 200 V to 400 V, (**b**) changing in input voltage from 400 V to 200 V, and (**c**) the output current, flying inductor current, input voltage, and output voltage at the input voltage of 400 V and step change at output power from 1 kW to 2 kW.

6. Main Design Challenges

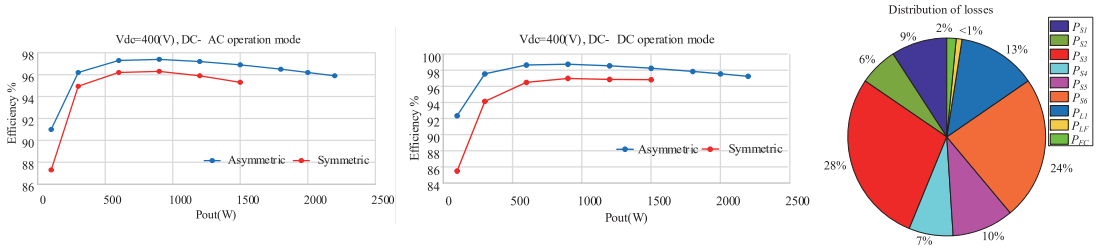
This section is devoted to the feasibility study of the selected converter for experimental verification. The unique feature of the FI power converter is that it has a continuous current in the inductor-charging path, unlike SC and FC power converters where the capacitor charge current is discrete. This requires the availability of a path to allow the inductor current to flow. Therefore, the biggest challenge in an FI converter is to ensure a smooth transition between the switches, which can be achieved through appropriate tuning of the dead time. This issue becomes more complicated when using a four-quadrant power switches arrangement, where the anti-parallel diode of each power switch is blocked by the other power switch.

If the dead time between the switches is too high, the inductor current will be obstructed for a brief period, leading to a substantial voltage surge across the switches. This surge will increase switching losses, decrease efficiency, and may harm the switches. To avoid this voltage spike issue, a snubber capacitor and varistor can be used as a solution, but this will add extra components, increase costs, and create additional losses. When the dead time between the switches is too low, the power switches will be in the on state, creating a quasi-short circuit. Although this limits the voltage surge across the switches, it also increases conduction losses and reduces efficiency, resulting in an increase in input current. Therefore, it is important to balance conduction losses and switching losses by finding an optimal dead-time value. This can be achieved by setting the dead time to different values and measuring efficiency using a power analyzer. Once the optimal point is found, the microcontroller can be used to adjust the dead time to the exact value.

The efficiency curve of the dual-purpose DC-DC/AC power converter operating in DC-AC mode with a 400 V input voltage is depicted in Figure 15a. The efficiency diagram is presented in two modes: buck–boost (symmetric) and buck (asymmetric). From the figure, it is evident that the efficiency is higher in the buck mode compared to the buck–boost mode. By examining Figure 15a, it is apparent that the maximum efficiency for an output power of 0.8 kW is 97.5% in buck mode and 96.4% in buck–boost mode. In addition to Figure 15a, Figure 15b depicts the efficiency curves of the selected converter in DC-DC operating mode with a 400 V input voltage. It is evident from this figure that the maximum efficiency at an output power of 1 kW is approximately 98.6% for the buck operation state and about 97% for the buck–boost mode.

The recorded efficiency was based on the proper dead-time tuning. According to Figure 6, during the positive half cycle, the inductor undergoes a charging process via S_5 and a discharging process via S_6. In contrast, during the negative half cycle, the charging and discharging of the inductor are conducted through S_4 and S_6, respectively. To ensure that the current in the inductor is continuous while transitioning between the charging and discharging modes, it is imperative to establish an appropriate dead time between S_5 and S_6 and between S_4 and S_6. However, since the SiC power switches have inherent delays,

as well as additional delays imposed by the gate driver, a dead time of zero is optimal for these mentioned power switches. On the other hand, the optimum dead time between other power switches has been determined to be 180 nS.



(**a**) (**b**) (**c**)

Figure 15. Experimental efficiency curves for 400 V input voltage: (**a**) DC-AC operation, (**b**) DC-DC operation, and (**c**) pie chart of the losses of each of the converter elements as a percentage.

Figure 15c displays a pie chart indicating the percentage of losses for each converter element. The power losses of power switches are the sum of P_{CON} (as written in (3)), and the switching losses (P_{SW}) in (28) in which I_S and Vs indicate the current and voltage stress of *ith* power switch, and N is the number of the used power switches. The conduction losses of the used inductors and the output filter capacitor are written in (29) and (30), respectively. In these equations, ESR_L, $I_{rms,L}$, ESR_C, and $I_{rms,C}$ refer to the Equivalent Series Resistance of an inductor, RMS current of an inductor, the Equivalent Series Resistance of the filter capacitor, and RMS current of the filter capacitor, respectively. Table 3 gives additional information to calculate the power losses of each component.

$$P_{SW} \cong \sum_{i=1}^{N_S} \langle \hat{i}_{Si} . \hat{v}_{Si} \rangle_T. \tag{28}$$

$$P_{Con,L} = ESR_L \times I^2{}_{rms,L}. \tag{29}$$

$$P_{Con,C} = ESR_C \times I^2{}_{rms,C}. \tag{30}$$

Table 3. Parameters for power loss calculation.

Parameters	Values
input voltage (V_{IN})	200 V
peak value of the output voltage (V_{out})	325 V
switching frequency (fs)	25 kHz
average output power (P_{out})	1 kW
on-state resistance of power switch	0.028 Ω
equivalent series resistance of FI	0.02 Ω
equivalent series resistance of output filter inductor	0.01 Ω
equivalent series resistance of output filter capacitor	0.01 Ω

7. Conclusions

In this paper, common-ground architecture was considered as a suitable solution for leakage current suppression in dual-purpose DC-DC/AC power converters. A comparative analysis was performed between several dual-purpose common-ground DC-DC/AC power converters. The comparison methodology was described comprehensively and the results were shown in the format of a radar chart illustrating the per unit values of W_C, W_L, TSV,

P_{CON}, and N_{SW} of each structure. Each solution has pros and cons. At the same time, FI solutions have significant magnetics but small capacitors due to the single-stage conversion.

A recently introduced power converter, as a family of novel FI power converters, was selected to be discussed as a dual-purpose DC-DC/AC common-ground solution with experimental verification. It uses a FI to store energy and pumps it to the output and is capable of operating as a buck and buck–boost converter. The operating modes were analyzed and the components design was discussed. In order to evaluate and show the accuracy of the selected converter, the experimental results in DC-DC and DC-AC modes were presented and analyzed. Finally, the design challenges in the selected topology were considered, and the efficiency and the loss distribution were analyzed. As a conclusion, the research team recommends solutions presented in [9,25,27] for practical applications due to the absence of four-quadrant switches and decent figure of merit.

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Data Availability Statement: The data used in this study are publicly available and sources are referred.

Conflicts of Interest: The authors declare no conflict of interest.

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Back-to-Back Energy Router Based on Common-Ground Inverters

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***Abstract*—With the increase of domestic generation resources (mainly photovoltaic), and the use of storage systems in many buildings, the utilization of the dc system along with ac system is being developed. For this purpose, energy routers with multiple ac and dc ports are employed. By the way, there are not enough standards to integrate the dc systems into the ac grid and safety considerations are still a problem. Many studies suggest the use of an isolated system, but isolation comes with increased volume and cost. This paper proposes an energy router based on a back-to-back structure with common-ground inverters. Connecting the neutral wire of the ac system to the negative port of the dc link eliminates leakage currents and ensures safety. The proposed energy router uses two common-ground inverters. Each inverter has five switches and has the ability to increase/decrease the voltage and also operate in both directions. The operation mode of the common-ground inverter has been investigated and the simulation results using PLECS confirm the accuracy of the overall structure and benefits compared to classical H-bridge inverter.**

Keywords—— Energy router, non-isolated, common-ground inverters, back-to-back structure.

I. Introduction

Due to the increasing integration of distributed generation resources in the domestic and distribution sector, the nature of the distribution system is changing from just consumer to generation and consumption. New buildings usually have photovoltaic (PV) production along with a storage system. These buildings can act like nanogrid since they have production, storage, and consumption and can work independently or in grid-connected mode. Usually in smart new buildings, the goal is to realize the concept of nearly-zero energy buildings (NZEB) and minimize the power drawn from the grid [1]. Considering that PV, storage system, and many loads work with dc power, the overall system can have dc and ac outlets and work as a dc or hybrid nanogrid [2].

Moving towards dc and hybrid systems is one of the topics of interest today which is being developed with the aim of higher overall efficiency. By using the dc system, higher efficiency will be achieved due to the reduced power conversion steps and higher efficiency of dc-dc converter [3]. In order to integrate the dc systems with the ac grid, standards have been proposed in recent years[4]. These standards do not yet cover all cases and are not comprehensive. In this regard, many studies have found it necessary to use an isolated system for safety and higher reliability [5], while isolation increases the size and volume. Regarding the lack of sufficient standards for this integration and grounding considerations, it is necessary to investigate other solutions as well.

In hybrid micro/nanogrid, energy router (ER) has been introduced and developed in the last decade. ER is an interface converter between ac and dc systems. This smart multi-port converter has the ability to manage and optimize energy flow between production, storage system and consumption [6]. ER can feed dc and ac loads and provide ancillary services to the grid. Various structures have been proposed for ER. In the high-power range, a three-stage power converter based on a solid-state transformer (SST) in the middle stage is proposed [7]. In the low power range, non-isolated hybrid inverters and back-to-back (B2B) structures are among the most prominent solutions [8], [9].

In the hybrid inverter, PV, storage, and dc loads are connected to the dc port, while ac loads are directly connected to the point of common coupling (PCC). In case of a fault in this structure, in either the grid or ac load, the other part is also affected. In the B2B structure, this problem has been solved. Due to the presence of the main dc link between two inverters, the ac loads of the building are detached from the grid. In different studies, this structure has been examined from different points of view. In [10], a control method is presented to control the grid-side inverter with the aim of controlling active and reactive power and compensating current harmonics, while in [11], the aim is to provide a control method based on model predictive control (MPC) to control the load-side inverter. Other studies have dealt with dc-link voltage control or charge/discharge current control of the storage systems [12]. In addition to the research conducted on ER based on hybrid inverters or B2B structures that investigated different aspects, studies have also focused on presenting new or isolated structures [13], [14].

In this regard, presenting new structures or modifying existed with the aim of improving ER performance is one of the leading research paths. As mentioned, in the hybrid inverter and B2B structure, the inverter has a conventional non-isolated structure (mainly H-bridge). Due to the lack of isolation and the presence of PV in the dc link, leakage current and safety issues should be resolved. This study proposes the B2B structure of an ER with common-ground inverters. Connecting the negative port of the dc link to the neutral wires of both inverters can solve the problems associated with safety and leakage current. Fig. 1 shows the general view of the proposed method with the common-ground concept. As seen

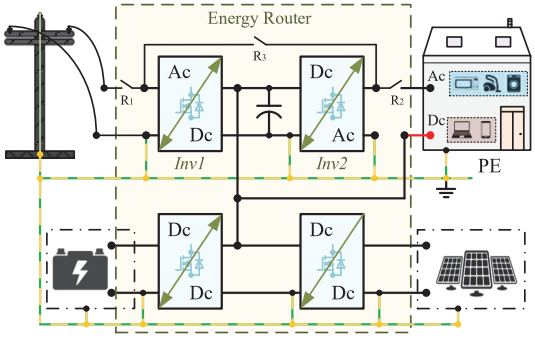

Fig. 1. Proposed energy router structure with grounding connections.

in Fig.1, the negative port of the dc link, the neutral wires of inverters, and the body of the equipment are all connected to each other and grounded. The use of relays R1 to R3 is also considered for switching between on-grid or off-grid states, isolating ac load, or parallel operation and load sharing of inverters, respectively.

Many studies have been reviewed to choose an appropriate common-ground inverter for this stricture [15]. As an example, a family of four-switch structures has been proposed in [16]. This structure work based on flying capacitors and have relatively simple modulation but with problems in bidirectional operation. In the rectification performance, they act as a half-bridge rectifier. Five switches switched capacitor is also proposed in [17]. This structure is also associated with problems caused by capacitor inrush current and switch current stress in the high-power range. Another common-ground inverter based on multilevel structures is presented in [18], which has more switches and relatively complex modulation. Single-stage buck-boost inverters based on common-ground inverters can also be a suitable option for this replacement [19]. In [20], a structure with five switches, an inductor, and a capacitor is provided, which has the ability to increase and decrease the voltage and can work bi-directionally. Regarding the benefits of this structure, here, this common-ground inverter has been used in the overall structure of the ER and its performance has been investigated in different operating conditions. The following parts will investigate this structure; in part II the structure of the alternative inverter and its operation is briefly described. In section III the overall structure of ER with common-ground inverters is examined. In part IV simulation results verify the performance of ER. Finally, the conclusion is added in part V.

II. Common-Ground Inverter

Transformerless inverters are an interesting option for PV applications due to their smaller volume and weight and subsequently lower cost. But they face a challenge due to safety issues related to leakage current. Different structures and different modulation methods for leakage current were presented and each of them reduced the leakage current to some extent [21]. Due to the fact that in the common-ground structure, the negative port of dc is directly connected to the neutral wire of ac, the parasitic capacitor is bypassed and the common mode voltage is clamped to zero. Therefore, the leakage current can be targeted. Hence, common-ground structures are very promising in PV applications.

In existing B2B structures, conventional structures (mainly H-bridge) are used for dc-ac conversion. Due to the absence of isolation, the problems caused by leakage current and safety issues still exist. In addition, this kind of inverter works only in a step-down manner and does not have the ability to increase voltage. Therefore, a suitable alternative should be found for these inverters. Fig. 2 shows the inverter intended to be replaced with conventional structures. This common-ground inverter uses five switches, an inductor, and a capacitor, and also has the ability to increase/decrease the voltage. In this figure, the input and output passive filter elements are also displayed.

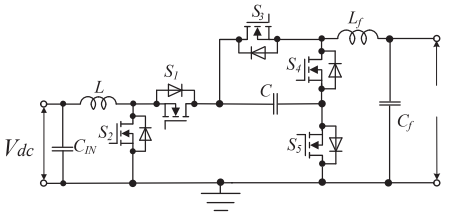

Fig. 2. The structure of the common-ground inverter intended for use in ER structure introduced in [20].

A. Operating Principle

Four operating modes including two zero modes, one positive mode, and one negative mode in the intended inverter are shown in Fig. 3. The output voltage is positive in mode A, zero in modes B and C, and negative in mode D. Positive and zero modes occur in positive half cycles and negative and zero modes occur in negative half cycles. In states A, B and D, the inductor is in the charging state, and in state C, the inductor is discharged. One advantage of this structure is the fixed duty cycle for boost operation. A detailed modulation strategy can be found in [20].

In this converter, the step-up part works according to the boost converter with a duty cycle of D. Therefore, the ratio of capacitor voltage to the dc input voltage is equal to:

$$V_C = \frac{1}{1-D} V_{dc}\,, \tag{1}$$

where D in this converter is the duty cycle of the boost part and corresponds to S2, which is responsible for boosting part of the converter. The output ac voltage is also as:

$$V_o = M V_C \sin(\omega t)\,, \tag{2}$$

where M is the modulation index and corresponds to the amplitude of the sine wave with the same frequency as the output voltage. Also, the peak of fundamental ac output is:

$$V_{o,\max} = M V_C\,. \tag{3}$$

Finally, the ac to dc gain is expressed as:

$$G = \frac{V_{o,\max}}{V_{dc}} = \frac{M}{1-D}\,. \tag{4}$$

In the modulation of this converter, D is always greater than M. After calculating M and D for the desired output, these values should be the output of the control system to produce PWM Pulses. Having D and M, four operating states of Fig, 3 are produced through the modulator as described in [20].

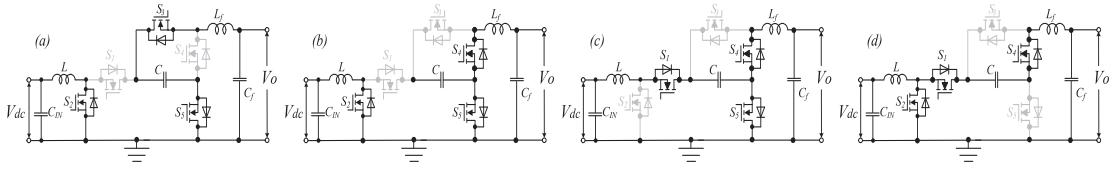

Fig. 3. Operating modes of the common-ground inverter (a) State A: L is charging, Vo=Vc. (b) State B: L is charging, Vo=0. (c) State C: L is discharging, Vo=0. (d) State D: L is charging, Vo=-Vc.

B. Passive components considerations

As previously mentioned, one of the advantages of this common-ground inverter is the fixed duty cycle. Then to calculate the inductor and capacitor, the same regular relations as for the boost converter can be applied. In each half cycle, the inductor is charged in two operating modes and discharged in another operating mode (mode C). Therefore, the following relations 5 and 6 can be used to calculate the inductor and capacitor according to the design limitations of the current ripple of the inductor and the voltage ripple of the capacitor.

$$L = \frac{V_{dc} D}{2\Delta I_L f_s}, \tag{5}$$

$$C = \frac{V_C D}{R f_s \Delta V_C}. \tag{6}$$

It should be added that the inductor current has a high-frequency ripple proportional to the switching frequency, which corresponds to equation 5. Also, according to the ac output, the inductor current corresponds to the absolute value of the load current. Similar situation also exists for capacitor voltage.

III. Energy Router with Common-Ground Inverters

Fig. 4 shows the overall structure of ER with two common-ground inverters along with their control blocks. It consists of the following blocks: grid-side inverter (*Inv1*) and LCL filter, load-side inverter (*Inv2*) and LCL filter, PV interface converter, and interface converter for battery storage.

In this structure, the negative port of the dc link and the neutral wires of both inverters are connected together. *Inv1* is located on the grid side and should be able to work bi-directionally. It means that it should draw power from the grid or inject power into it. To control *Inv1*, two phase-lock-loops (PLL) and a PI controller along with a proportional resonance controller are used to finally produce *M* and *D* required by the inverter. PLL1 samples grid voltage and provides synchronization to the primary grid. Additional PLL2 sampling output current (I_o), provides a pure sinusoidal reference current that is equal to the fundamental harmonic of the output current. It will provide only a sinusoidal grid current under any shape of the output current. For these two PLLs, the traditional second-order generalized integrator (SOGI) regulator is used. The grid side reference current is derived by means of a simple proportional-integral (PI) controller, in combination with the instantaneous value of the output current. This provides the instantaneous power balance between the output side and the grid side, which, in turn, mitigates the power ripple across the dc-link capacitor and improves the dynamic of the system. Finally, a conventional proportional resonant (PR) is used for grid current control [22]. On the ac-loads side, *Inv2* also uses a common-ground structure. For *Inv2*, there is an MPC controller to generate the modulation index *M* and a PI controller to generate *D*. In the MPC controller, the cost function is defined in such a way as to minimize the changes in the output voltage of the inverter near the reference output voltage under any kind of loads. As was demonstrated in [23] MPC becomes a feasible instrument for power electronics applications. It should also be mentioned, by applying the proportional coefficient, the condition *D>M* should always be satisfied in both controllers of *Inv1* and *Inv2*. The PV and storage system are also connected to the dc link through their respective dc-dc converters, and each has its own controllers, which is not the focus of the discussion here. Here, the goal is to focus on the operation of two inverters in grid-connected mode and power exchanges between the load, the dc link, and the grid.

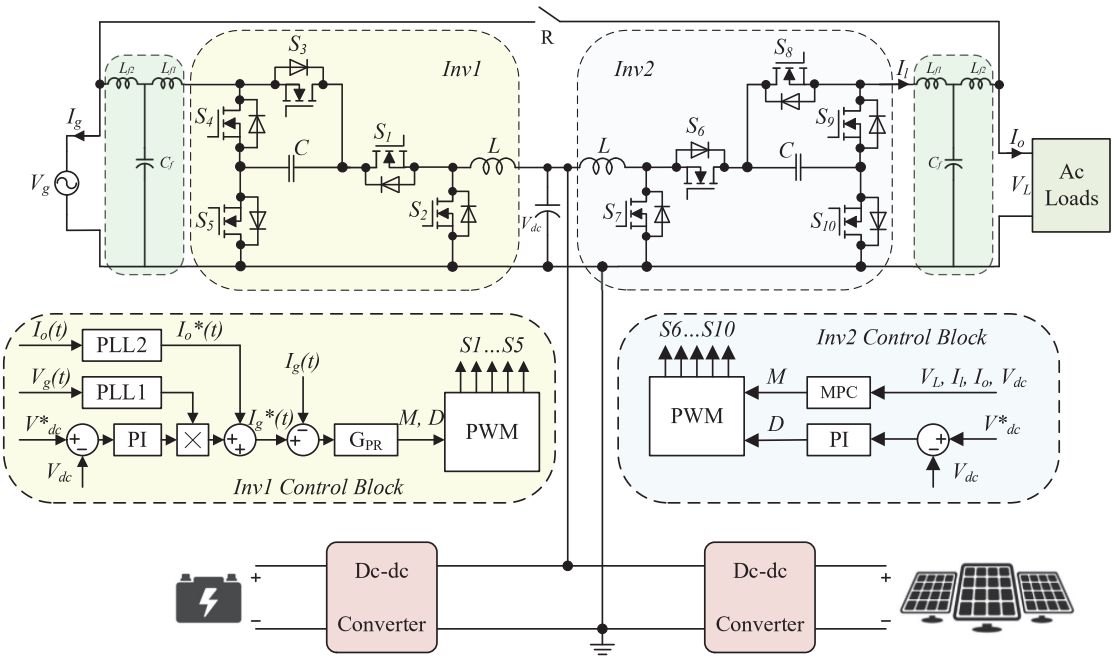

Fig. 4. General schematic of ER with two common-ground inverters and their control block.

IV. Simulation Verification

For the investigation of the performance of two common-ground inverters and comparing them with conventional inverters in ER structure, PLECS software has been used. Firstly, the parameters of passive components were calculated by means of the presented above considerations (1) to (6). Table I summarizes the simulation parameters. In the first part, the performance of the proposed structure has been examined in different situations. Then, the THD of the grid current in the states of power injection/receiving in the proposed structure has been compared with the conventional structure.

A. General performance

First, the performance of overall system in the condition of changing the output load (ac loads) is investigated. To simplify and reduce the situations under consideration in these simulations, it is assumed that constant power is transferred from the battery and PV side to the dc link in this section. It is assumed that the power of 3000 W is given to the dc link from the PV and battery side. At the moment t = 0.7 s, the output load increases from 1000 W to 2000 W. With this increase, the output load current (I_o) increases. Then, overall controllers of the system perform the necessary corrections for stable operation. Fig. 5 shows the dc link voltage, *Inv1* and *Inv2* output voltage and tenfold current (for a better view). As it can be seen, with the increase of the output load, the voltage of the dc link will drop slightly, but it will still be within the permissible range. (Fig. 5a). For the output of *Inv2*, it can also be seen in Fig. 5b that at the moment of load increase, the inverter current has increased (doubled) and the output voltage has seen a very small drop (between 2-3 V) at this moment. Therefore, as can be seen, after this load change, the control system was able to keep the dc link and output voltage of *Inv2* within the allowed range.

On the other hand, the power injected into the grid is the difference between dc link power and output load power. At the moment of increasing the output load from 1000 W to 2000 W, the power injected into the grid will decrease due to the constant power of the dc link. Fig. 5c shows the grid-side voltage and tenfold current. At the moment t=0.7 s, with the increase of the output load, the power injected into the grid has decreased as can be seen. In this figure, the voltage and current before and after changing the output load are in phase and the power factor is unity. Also, the current injected into the grid is sinusoidal and has the minimum possible distortion.

TABLE I. Simulation Parameters.

Parameter's name	Value	Units
Output Voltage, V_L	230	V
Dc-link voltage, V_{dc}	400	V
Dc-link capacitor	2000	uF
LCL filter inductance, $L_{f1(Inv1)}$ and $L_{f2(Inv2)}$	1.4	mH
LCL filter capacitance, C_f	9	uF
LCL filter inductance, $L_{2(Inv1)}$ and $L_{2(Inv2)}$	0.6	mH
Switching frequency, f_s	10	kHz
Inverters inductors, L	1	mH
Inverters capacitors, C	200	uF

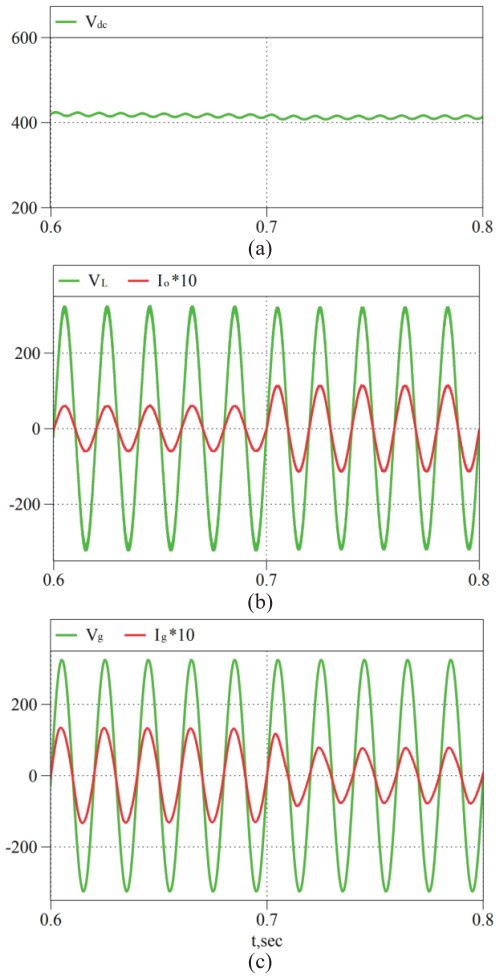

Fig. 5. Simulation of changing the load from 1000 W to 2000 W at t=0.7 s for ER with common ground inverters: dc-link V_{dc} (a), load side V_L and I_o (b), grid side V_g and I_g (c).

Considering that the power of the PV and battery is considered to be 3000 W, if the load power is greater than this value, the *Inv1* on the grid side should draw the power difference from the grid to feed the output load. To check this situation, it is assumed that the output load was 2000 W at the beginning, and then at the moment t=0.7 s, the output load increases to 6000 W. Due to the presence of 3000 W of power in the dc link, *Inv1* should receive the required power difference from the grid and transfer it to the output load. Fig. 6 shows the voltage and current of the grid side for this scenario. As can be seen, the extra power available in the dc link (while feeding ac loads) has been injected into the grid before t=0.7 s. With the increase of the output load at t=0.7 s, the power available in the dc link alone cannot feed the ac loads. Then the grid current direction is changed to supply the output load, and power is drawn from the grid. The simulation in this case also confirms the correctness of the bidirectional operation of the alternative inverter. Another point is that in the case of power injection into the grid, the voltage and current are in phase and the power factor is unity, and when the current direction changes, the voltage and current will

have a phase difference of 180 degrees and the power factor will also be close to unity.

For the situation under non-linear loads, the performance of the proposed structure is also considered. Similar to the first case, the power of 3000 W is considered in the dc link. The load-side *Inv2* draws 1000 W power for household appliances. In t=0.7 s, a non-linear rectification load of 1000 W is added to the output. With the addition of this load, the current waveform will be distorted. But as seen in Fig. 7, the MPC controller produces an output voltage with low distortion. In this case, the THD of the output voltage is close to 3.5%, while in completely similar conditions of non-linear load the application using the H-bridge inverter, the THD value will be close to 3%. Therefore, it can be deduced that the proposed structure has an acceptable performance under non-linear loads.

B. *Comparison of the THD of grid current in the proposed structure with the H-bridge-based structure*

To further investigate the performance of the proposed ER, the THD of the grid current has been investigated in two modes of using H-bridge inverters and common-ground inverters. This comparison is performed with the same conditions in switching frequency, LCL filter, etc. for both structures based on Table I. Here, the comparison has been made for two modes of power injection into the grid and power receiving from it at different power levels. PLECS simulation has been implemented to simulate both structures.

In the first case, to inject power into the grid, the output load power of *Inv2* is fixed at the low power of 250 W. The produced power in the dc link has been considered at different levels and comparison has been performed for two modes of using different inverters. Fig. 8 shows the value of THD in the mode of power injection to the grid for two structures of H-bridge-based (H-B) and common-ground-based (C-G). As can be seen, in all injected powers, with the use of the common-ground inverter, the THD of the current is less and with the increase of dc link power and subsequently the increase of injected power to the grid, the amount of THD slightly decreases. Also, in the H-bridge-based structure with the increase of injected power, THD will decrease. Of course, it should be kept in mind that the LCL filter in these structures is designed for a power range close to 5 kW, and performance at light loads is associated with an increase in THD.

In the second case, to check the condition when the power produced in the dc link is insufficient to supply the output loads, the performance of the B2B structures has been checked with H-bridge and common-ground inverters. In this situation, the output power in the dc link is considered fixed at 500 W and the output load power is at different levels. The results of the simulation for the THD of the grid current for H-bridge-based (H-B) and common-ground-based (C-G) structures are shown in Fig. 9. At low received power from the grid, both structures have relatively larger THD. Although in the H-bridge-based structure, this value is 7.5% and larger than in the common-ground-based structure. As can be seen, in this case also, as the power received from the grid increases, the THD value decreases for both structures and reaches very low values for the rated power. Of course, in this case, the performance of the H-bridge is better at high loads. It can also be concluded that the presented common-ground structure, has a better performance in inverter mode rather than rectification mode.

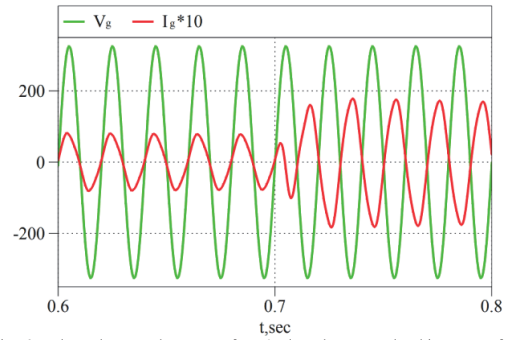

Fig. 6. The voltage and current of *Inv1* when the output load increases from 2000 W to 6000 W at t=0.7 s and the power of the dc link is 3000 W.

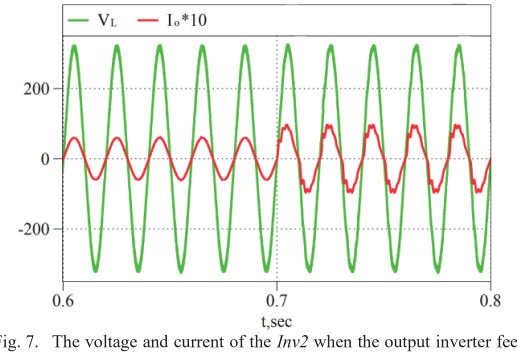

Fig. 7. The voltage and current of the *Inv2* when the output inverter feeds 1000 W and at t=0.7 s a non-linear rectification load of 1000 W is added.

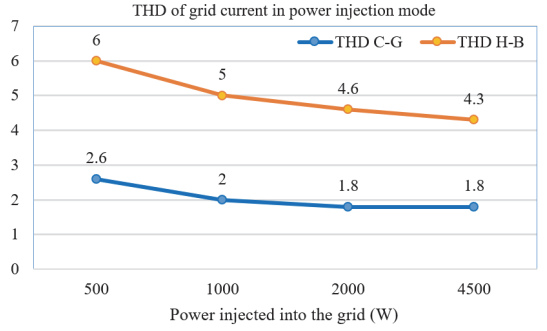

Fig. 8. Comparison of THD of grid current in the mode of power injection by using H-bridge inverters (H-B) and common-ground inverters (C-G).

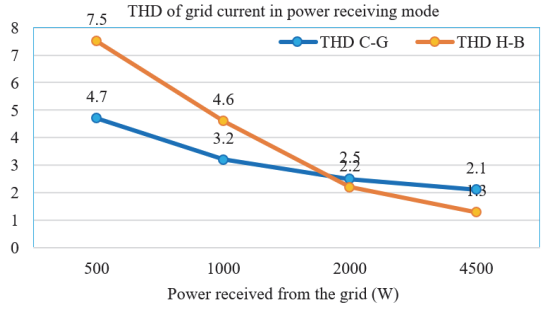

Fig. 9. Comparison of THD of grid current in the mode of the power receiving by using H-bridge inverters (H-B) and common-ground inverters (C-G).

To summarize, it should be mentioned that using the common-ground inverters in the general structure of ER can be a potential option. Solving problems caused by leakage current and safety and on the other hand, the flexibility of these inverters in the circuit structure, and voltage increase/decrease are among their features. Of course, other matters related to the design, size of passive elements, implementation, and general control of these converters should be carefully examined [24].

V. Conclusions

This paper presented a solution to mitigate leakage current and safety issues in non-isolated ER structures. By using common-ground inverters in a B2B structure of ER, the negative port of the dc link was connected to the neutral wires of the inverters to avoid the problems caused by leakage current and ensure safety. The results obtained from the simulation in different operating conditions, the correctness of the structure's performance in conditions including changing the output power, receiving or injecting power into the grid, and bidirectional operation were checked. The THD of the grid current was compared in both cases of using the H-bridge and the common-ground inverters, and the results confirmed the valid performance of the structure based on the common-ground inverters. These results confirm the good potential of this structure in cases of using non-isolated systems for the future of ER structure.

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A Novel Flying Inductor based Grid-Connected Inverter with Buck-Boost Ability

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***Abstract*- A single-phase single-stage flying inductor based buck-boost inverter (S^2FIB^2I) is presented in this paper. Operation in buck, boost and buck-boost modes gives the proposed topology the ability to inject power into the grid at a wide range of input voltages. In other words, the proposed inverter has a dynamic voltage gain. The direct connection of the negative terminal of the input source with the neutral terminal of the power grid causes that in photovoltaic applications, the problem of injecting even harmonics into the grid is solved and the leakage current is completely eliminated. The absence of electrolytic capacitors in the proposed converter increases the life and reliability of the system. Also, the ability to operate at non-unity power factor allows the proposed inverter to control the reactive power at its output terminals. Theoretical analysis, design of passive elements and 1 kW simulation results are given to prove the accuracy of the proposed inverter performance.**

Index Terms*- *Common ground topology, Flying inductor based inverter, Transformerless grid connected inverter, Buck-boost operation.

I. INTRODUCTION

Power electronic converters are widely used in renewable energy applications, especially in photovoltaic systems [1]-[6]. Among these, transformerless grid connected inverters are more popular and are used in residential and industrial scales [7]-[9]. Failure to use the transformer increases the power density and efficiency and reduces the cost and overall weight of the system, but removing the transformer in the grid-connected systems requires passing the grid codes in the electrical distribution systems [10]-[11]. Also, the removal of the transformer causes a leakage current due to the scattering capacitors of the solar panels, which according to the standard (VDE0216-1-1 IEEE), the amount of leakage current should be below 300 mA. In order to reduce the leakage current, H4 inverter with bidirectional modulation, H5 [12], improved H5 [13], H6 [14] and its family [15], HBZVR [16] and HERIC [17] are used. Although these inverters limit leakage current, they do not completely eliminate it. These structures also require a boost converter stage to be able to inject power into the grid at the input voltages below the peak of grid voltage. References [17]-[19] provide other structures for grid-connected inverters. The buck-boost capability of these structures makes it possible to inject power into the grid at a wide range of input voltages. In these structures, although the leakage current is reduced, it is still not completely eliminated. These structures also face limitations in reactive power control.

Recently, common ground topologies have come to the attention of researchers. Because in these structures, the scattering capacitors are completely bypassed and eliminate the leakage current from the system. In the references [20]-[22] the common ground topologies based on switch capacitor (SC) technology are presented. In these structures, the leakage current is completely eliminated. But the problem of these structures is the inability to boost voltage and also the capacitors in these structures have a high spike charge current. In references [23]-[26] various multilevel inverters are provided. These structures have no leakage current problem and also have voltage boosting capability. The problem with these structures is the presence of spike charge current of the capacitors and also their voltage gain is limited and usually have a constant value.

In the references [27]-[30] various flying inductor based structures are presented for grid connected inverters, which are in the form of a common ground and completely eliminate leakage current. Also, the buck-boost capability of these structures allows the transfer of power from the input source to the output grid in a wide range of input voltages without the need for an additional boost converter stage. Nevertheless, in these structures, the used inductor has a relatively large volume.

In this paper, a new topology based on flying inductor is presented, which is in the form of common ground, and causes the complete elimination of leakage current in photovoltaic systems. The buck-boost capability of the proposed inverter allows sing stage power processing to be performed in a wide range of input voltages. The proposed inverter also has the ability to control reactive power. The article is set as follows: Section II presents the proposed inverter and Section III describes operating modes. In Section IV, passive elements are designed, and the voltage and current stress of active elements are examined. In section V, the simulation results are presented and finally in VI, the conclusion is given.

I. Proposed Topology

The proposed single-phase single-stage flying inductor based inverter (S^2FIB^2I) is shown in Fig. 1. This converter is based on the flying inductor technique, and in one stage, the power is transferred from the input source to the grid. The dynamic voltage gain capability of the proposed inverter makes it possible to transfer power from the input dc source to the output grid in a wide range of input voltages. In other words, the proposed inverter has a buck-boost voltage capability. Unlike sc converters, which use electrolytic capacitors in the process of transferring power from the input source to the output load, here the flying inductor is used for the process of transferring power, which increases the reliability of the system and the life of the converter. In the proposed converter, the negative terminal of the input dc source is connected directly to the neutral terminal of ac grid. This feature is very important in photovoltaic systems and especially in grid connected inverters. Because it generally bypasses the scattering capacitor of photovoltaic panels and prevents the injection of dc current and even harmonics into the ac grid and improves the quality of injected power into the grid. Injecting reactive power into the power grid or absorbing reactive power from it in grid-connected systems is very important. In other words, performance in a non-unity power factor is a requirement of grid-connected systems, in which an inverter must be able to operate. The proposed inverter can control the reactive power at the point of common coupling (PCC) by operating on the leading and lagging power factors, without affecting the leakage current.

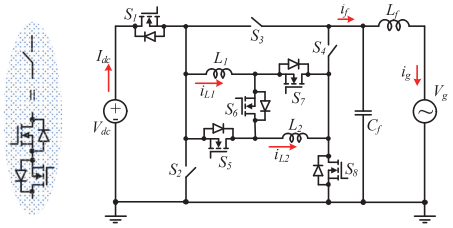

Fig. 1. Proposed single-phase single-stage flying inductor based buck-boost inverter.

III. Operation Modes of Proposed FIS^2B^2I

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According to Fig. 1, the proposed S^2FIB^2I consists of eight switches, two inductors and an output LC filter. Five switches are two-quadrant in which ordinary Si or SiC switches can be used. In three switches, the voltage needs to be blocked in two directions. Therefore, four-quadrant or RB-IGBT switches can be used for this purpose. If the proposed inverter operates as a buck-boost in both positive and negative half-cycles, then the current amplitudes of inductors L_1 and L_2 in the positive and negative half-cycles will be equal. In fact, these operating conditions are called symmetric modes. The proposed converter in the positive half-cycle can operate in buck and boost modes, depending on the value of input voltage. If the input voltage is higher than the instantaneous value of the output voltage, then the converter is in buck mode, and if the input voltage is less than the instantaneous value of the output voltage, then the converter is operating in boost mode. Also, if the input voltage is greater than the peak value of the output voltage, then the converter can operate the entire positive half-cycle interval in buck mode. These operating conditions cause the current amplitudes of inductors L_1 and L_2 to have different values in the positive and negative half cycles, which is called asymmetric mode. Symmetric and asymmetric operating modes are shown in Figs. 2 and 3, which are discussed below.

A. Symmetric State

1) *First Operation Mode:* The first operating mode in symmetric state is shown in Fig. 2(a). In this mode, the converter is in the positive half cycle of the power grid. Switches S_1, S_5, S_7 and S_8 are on, allowing inductors L_1 and L_2 to be charged in parallel from the input source. In addition, the output load current or the power grid closes its path through the capacitor C_f. Other switches are off in this mode. The blue path shows the charge current of the inductors and the red path shows the grid current. This mode is also known as active mode in the positive half cycle.

2) *Second Operation Mode:* The second operating mode is also in the positive half cycle of the power grid. In this mode, switches S_2, S_4 and S_6 are on and injecting the stored energy in inductors L_1 and L_2 into the output filter and the grid. Also in this mode, inductors L_1 and L_2 transfer their energy to the output in series with each other. In buck-boost mode, L_1 and L_2 act as energy storage sources. In other words, in one period of time they receive energy from the input source and in another period of time, they inject the stored energy towards the output. This mode is known as freewheeling mode in the positive half cycle. The equivalent circuit of the second operating mode is shown in Fig. 2(b).

3) *Third Operation Mode:* In the third operating mode, the proposed converter is in the negative half cycle. The output current direction in this case is opposite to the first and second operating modes, but still the current direction in inductors L_1 and L_2 are the same as the first and second operating modes. In this mode, switches S_1, S_5, S_7 and S_8 charge L_1 and L_2 in parallel from the input source when they turn on. This mode is known as active mode in the negative half cycle. The equivalent circuit of the third operating mode is shown in Fig. 2(c).

4) *Fourth Operation Mode:* The fourth operating mode, like the third operating mode, is in the negative half cycle. In this mode, the stored energy in inductors L_1 and L_2 is injected in series through the switches S_3, S_6 and S_8 to the output filter and power grid. This mode is also known as freewheeling mode in the negative half cycle. The equivalent circuit of the fourth operating mode is shown in Fig. 2(d).

B. Asymmetric State

In the asymmetric state, the proposed inverter is in buck or boost operating modes, which depends on the input voltage. Also, this mode is only for the positive half cycle of the power grid.

1) *First Operation Mode:* The first operating mode is shown in Fig. 3(a). In this mode, the input voltage is less than the instantaneous value of output voltage and the inverter is in boost mode.

Switches S_1, S_5, S_7 and S_8 charge inductors L_1 and L_2 in parallel from the input source. The grid current also closes its path through the capacitor C_f. This mode is also called active mode in the positive half cycle.

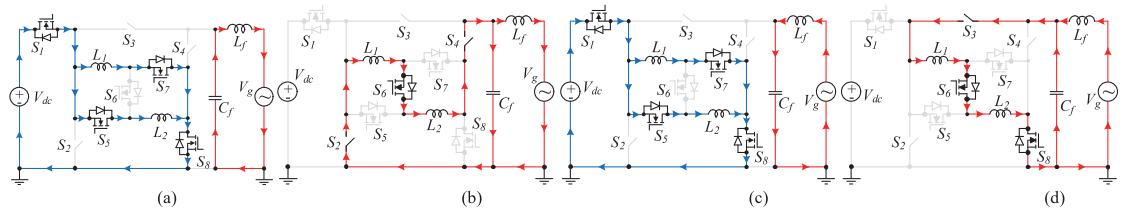

Fig. 2. Equivalent circuit of the proposed inverter in buck-boost operation mode: (a) active mode in the positive half cycle, (b) freewheeling mode in the positive half cycle, (c) active mode in the negative half cycle, and (d) freewheeling mode in the negative half cycle.

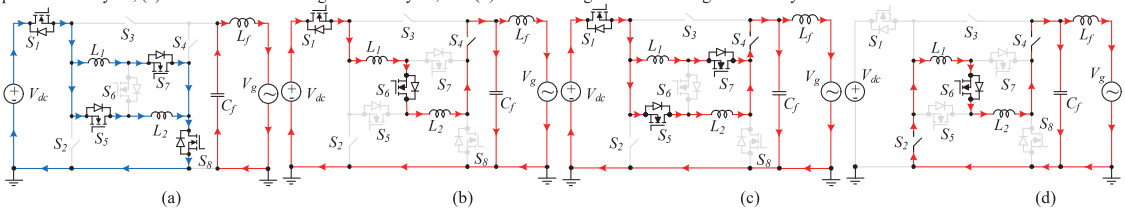

Fig. 3. Equivalent circuit of the proposed inverter in the buck and boost operation modes: (a) active mode in the boost state during the positive half cycle, (b) freewheeling mode in the boost state during the positive half cycle, (c) active mode in the buck state during the positive half cycle, and (d) freewheeling mode in the buck state during the positive half cycle.

2) *Second Operation Mode:* The second operating mode in asymmetric state is shown in Fig. 3(b). In this mode, like the first operating mode, the converter is in boost mode. When switches S_1, S_4 and S_6 are switched on, the stored energy inside the inductors L_1 and L_2 in series with the input voltage is transferred to the output filter and power grid. This mode is also called freewheeling mode.

3) *Third Operation Mode:* Since in the third operating mode, the input voltage is higher than the instantaneous value of the output voltage, so the proposed inverter operates in buck mode. In buck mode, despite boost and buck-boost modes, inductors L_1 and L_2 act as filters. This reduces the amplitude of the inductor current in the buck mode, less than the boost and buck-boost modes. The equivalent circuit of the third operating mode is shown in Fig. 3(c). In this figure, switches S_1, S_4, S_6 and S_7 are on and power is transferred from the input source to the output grid from through the inductors. This mode is also known as active mode in the positive half cycle.

4) *Fourth Operation Mode:* The fourth operating mode in asymmetric state is shown in Fig. 3(d). This mode, like the third operating mode, is in buck state. Also, this operating mode is known as freewheeling mode in the positive half cycle. The current of inductors L_1 and L_2 is transmitted in series by switches S_2, S_4 and S_6 to the output filter and power grid.

IV. Design Guidelines

In this section, the duty cycle of the proposed inverter in buck, boost and buck-boost operating modes is calculated. Next, the value of passive elements is calculated and finally the voltage and current stress of the switches are discussed.

A. Duty Cycle Valculation

Given that, the proposed inverter can be used in three operating modes buck, boost and buck-boost, so it is necessary to calculate the duty cycle for these three modes. The duty cycle in buck, boost and buck-boost modes is indicated by d_1, d_2 and d_3, respectively. Output voltage and current in unity power factor are expressed as follows:

$$v_g(t) = V_{o,\max} \sin \omega t \,, \tag{1}$$

$$i_g(t) = I_{o,\max} \sin \omega t \,. \tag{2}$$

Inductors L_1 and L_2 are equal in the proposed converter. By writing the volt-second balance law for each of the inductors and by simplifying it, the duty cycle for buck, boost and buck-boost modes is expressed as follows:

$$d_1(t) = \frac{v_g(t)}{2V_{dc} - v_g(t)} = \frac{V_{o,\max} \sin \omega t}{2V_{dc} - V_{o,\max} \sin \omega t}, \quad \textit{buck mode} \tag{3}$$

$$d_2(t) = \frac{v_g(t) - V_{dc}}{v_g(t) + V_{dc}} = \frac{V_{o,\max} \sin \omega t - V_{dc}}{V_{o,\max} \sin \omega t + V_{dc}}, \quad \textit{boost mode} \tag{4}$$

$$d_3(t) = \frac{v_g(t)}{2V_{dc} + v_g(t)} = \frac{V_{o,\max} \sin \omega t}{2V_{dc} + V_{o,\max} \sin \omega t}. \quad \textit{buck- boost mode} \tag{5}$$

B. Design of Flying Inductors L_1 & L_2

In this section, the value of inductors L_1 and L_2 is calculated. These inductors are equal to each other. Due to the fact that the inductor current ripple in the buck-boost converter is more than the buck and boost converter, so in this proposed converter, the flying inductors current ripple in buck-boost operating mode is more than the buck and boost operating modes. As a result, the current ripple equation for inductor L_1 is written in buck-boost mode. The current ripple of inductor L_1 is expressed as follows:

$$\Delta i_{L1} = \frac{d_3 \cdot V_{dc}}{L_1 \cdot f_S}. \tag{6}$$

In the relation (6), f_S is the switching frequency of the converter. The maximum current ripple of inductor L_1 is expressed as follows according to the percentage of current ripple and also based on the output power in buck-boost operating mode:

$$\Delta I_{L1,\max} = K_{L1} \cdot \frac{\left(1 + D_{3,\max}\right) \cdot P_o}{\left(1 - D_{3,\max}\right) \cdot V_{o,\max}}. \tag{7}$$

In the above relation, P_o is the average value of output power, $V_{o,max}$ is the peak of output voltage, K_{L1} is the percentage of inductor L_1 current ripple and $D_{3,max}$ is the maximum duty cycle in buck-boost operating mode, which is defined as follows:

$$D_{3,\max} = \frac{V_{o,\max}}{2V_{dc} + V_{o,\max}}. \quad (8)$$

Finally, by placing relations (5), (7) and (8) in (6), the value of inductor L_1 is obtained as follows:

$$L_1 = \frac{V_{dc}^2 \cdot V_{o,\max}^2}{K_{L1} \cdot \left(2V_{dc} + V_{o,\max}\right) \cdot \left(V_{dc} + V_{o,\max}\right) \cdot P_o \cdot f_S}. \quad (9)$$

The value of inductor L_2 is also obtained from the above relation.

C. Design of Output Capacitor C_f

Equation (2) shows the grid current in the unity power factor. As mentioned earlier, the flying inductors have a higher current ripple in the buck-boost mode than the other modes, which means that the voltage ripple of output capacitor C_f is also higher in the buck-boost mode than other modes. Therefore, the C_f is calculated for the buck-boost operating mode. According to Fig. 2(a) the current passing through the capacitor C_f is equal to the grid current. Therefore, the voltage ripple of this capacitor is expressed as follows.

$$\Delta v_{Cf} = \frac{d_3 \cdot i_g}{C_f \cdot f_S}. \quad (10)$$

By placing relations (2) and (5) in (10), the capacitance of C_f under maximum voltage ripple conditions is calculated as follows:

$$C_f = \frac{2P_o}{\Delta V_{Cf,\max} \cdot f_S \left(2V_{dc} + V_{o,\max}\right)}. \quad (11)$$

D. Current and Voltage Stress Analysis

In order to calculate the current stress of the switches, it is necessary to calculate the maximum current passing through the inductors. The maximum current passing through each of the inductors L_1 and L_2 is calculated as follows:

$$I_{L1,peak} = \frac{\left(1 + D_{3,\max}\right) \cdot I_{o,\max}}{2(1 - D_{3,\max})} + \frac{\Delta I_{L1,\max}}{2}. \quad (12)$$

By placing relations (6) and (8) in (12), the peak value of current of inductor L_1 based on the value of output power is expressed as follows:

$$I_{L1,peak} = \frac{\left(V_{dc} + V_{o,\max}\right) \cdot P_o}{V_{dc} \cdot V_{o,\max}} + \frac{V_{dc} \cdot V_{o,\max}}{2L_1 \cdot f_s \cdot \left(2V_{dc} + V_{o,\max}\right)}. \quad (13)$$

Finally, the current stress of the switches is expressed as follows:

$$I_{S2} = I_{S3} = I_{S5} = I_{S6} = I_{S7} = I_{L1,peak}, \quad (14)$$

$$I_{S1} = I_{S4} = I_{S8} = 2I_{L1,peak}. \quad (15)$$

The current stress of switches S_2, S_3, S_5, S_6 and S_7 is equal to the peak current of inductors L_1 or L_2, while the current stress of switches S_1, S_4 and S_8 is equal to the sum of currents of inductors L_1 and L_2.

Finally, the voltage stress of the switches is as follows:

$$V_{S1} = V_{S3} = V_{dc} + V_{o,\max}, \quad (16)$$

$$V_{S2} = V_{S4} = V_{S8} = V_{o,\max}, \quad (17)$$

$$V_{S6} = V_{dc}, \quad (18)$$

$$V_{S5} = V_{S7} = \frac{V_{o,\max}}{2}. \quad (19)$$

According to the above equations, it can be seen that the maximum voltage stress is related to switches S_1 and S_3.

V. Simulation Results

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In order to show the correct operation of the proposed inverter, a number of simulation results are given in this section. The parameters used in the simulation environment are shown in Table I. MATLAB Simulink environment is also used to simulate the proposed inverter. During simulation, the powergui value is selected as 1e-8. In addition, the simulation results are shown only in buck- boost mode for both positive and negative half cycles. Fig. 4 shows the voltage stress of the switches per 200 V input voltage and 230 V rms output voltage. Maximum voltage stress between the switches is related to switches S_1 and S_3, which are equal to the sum of input and output voltages and are shown in Figs. 4(a) and (c), respectively. Also, the lowest voltage stress is related to switches S_5 and S_7, each of which is half of the output voltage and is shown in Figs. 4(e) and (g), respectively. Fig. 5 shows the current stress of the switches. According to Figs. 5 (b)- (g), it can be seen that the current stress of S_2-S_7 switches is equal to the current of inductors L_1 or L_2. Also, the currents of inductors L_1 and L_2 are equal. While the current stress of switches S_1 and S_8 is twice the current stress of other switches and is equal to the sum of currents of inductors L_1 and L_2. Because these switches charge the inductors L_1 and L_2 in parallel by the input source. Finally, the output voltage and current of the proposed inverter along with the current of inductors L_1 and L_2 are shown in Fig. 6. Fig. 6(a) shows the proposed inverter output voltage and current. In this case, the output power is 1 kW and the output load is in unity power factor.

Fig. 6(b) shows the current of inductor L_1. Since in this figure the output load is in unity power factor, so it causes the current of inductor L_1 to have a positive value in the whole time interval. Given that the proposed inverter also has the ability to control reactive power, so to show this feature, Figs. 6(c) and (d) are given. Fig. 6(c) shows the output voltage and current in the leading power factor. Fig. 6(d) also shows the current of inductor L_1.

It can be seen from Fig. 6(d) that in a period of time, the current of inductor L_1 has a negative value, in other words, in this period of time, the current is returned to the input source, and the reason for this is due to the control of reactive power. Also, in order to show the performance of the proposed inverter in lagging power factor mode, Fig. 6(e) is given and this figure shows the output voltage and current. Fig. 6(f) also shows the current of inductor L_1 and the negative value of the current of this figure is due to the control of reactive power in the lagging power factor mode.

TABLE. I. PARAMETER USED FOR SIMULATION THE PROPOSED TOPOLOGY.

V_{in}	V_{out}	f_S	L_1 & L_2	L_f	C_f	P_{out}
200 V	230V rms	50 kHz	150 uH	100 uH	3.3uF	1 kW

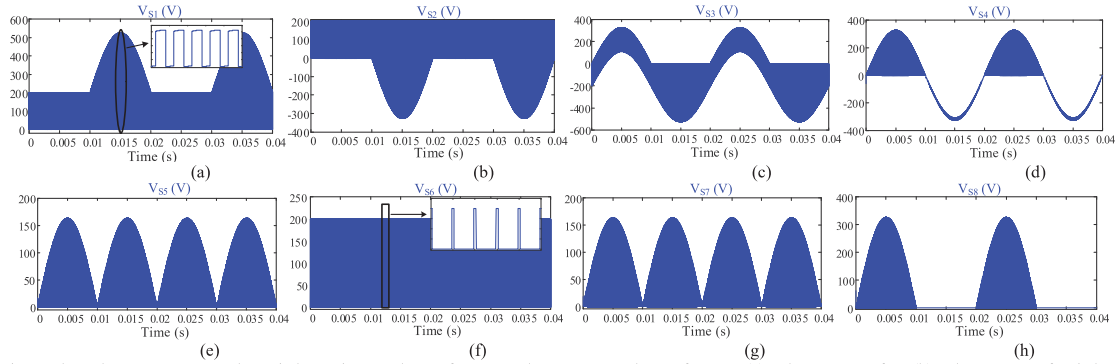

Fig. 4. The voltage stress across the switches at input voltage of 200 V and rms output voltage of 230 V: (a) voltage stress of S_1, (b) voltage stress of switch S_2, (c) voltage stress of S_3, (d) voltage stress of S_4, (e) voltage stress of S_5, (f) voltage stress of S_6, (g) voltage stress of S_7, and (h) voltage stress of S_8.

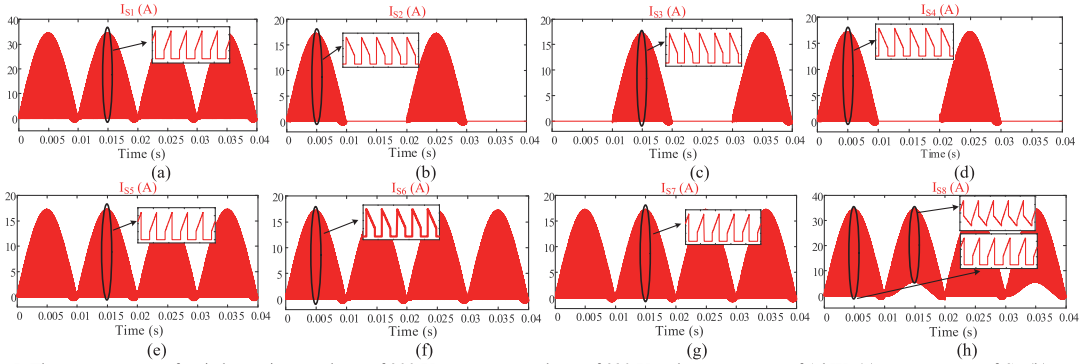

Fig. 5. The current stress of switches at input voltage of 200 V, rms output voltage of 230 V and output power of 1 kW. (a) current stress of S_1, (b) current stress of S_2, (c) current stress of S_3, (d) current stress of S_4, (e) current stress of S_5, (f) current stress of S_6, (g) current stress of S_7, and (h) current stress of S_8.

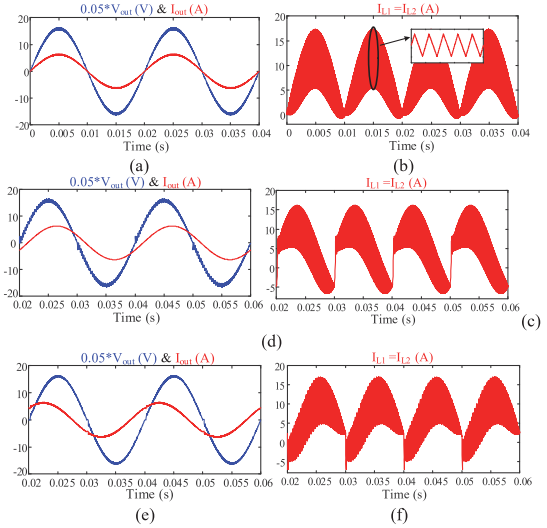

Fig. 6. The output voltage, output current and flying inductors' current at input voltage of 200 V, rms output voltage of 230 V, and output power of 1 kVA: (a) output voltage and current at unity power factor, (b) current of inductors L_1 and L_2 at unity power factor, (c) output voltage and current at leading power factor, (d) current of L_1 and L_2 at leading power factor, (e) output voltage and current at lagging power factor, and (h) current of inductor L_1 and L_2 at lagging power factor.

VI. Conclusions

In this paper, a new topology for the grid-connected inverter is introduced, which is based on the flying inductor. The buck, boost and buck-boost capability of the proposed inverter makes it possible to inject power from the input source to the output grid in a wide range of input voltages. Also, the single-stage power processing capability of the proposed inverter makes it possible to achieve high efficiency, and this is suitable for commercial applications. The absence of an electrolytic capacitor in the proposed inverter can increase the reliability and service life of the system. Also, the same connection between the negative terminal of input source and the neutral terminal of ac grid completely eliminates the system leakage current in pv applications. In addition, the possibility of return current to the input source makes it possible to control the reactive power for the proposed converter. Finally, in order to show the correct operation of the proposed inverter, the simulation results are shown at an output power of 1 kW.

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Model Predictive Control of A Single-Stage Flying Inductor Based Buck-Boost Grid-Connected Common-Ground Inverter

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***Abstract*— In this paper, the Model Predictive Control (MPC), of a transformer-less single-phase single-stage grid-tied current-source inverter is presented. The common-grounding feature of this converter increases its reliability and suppresses the leakage current. Moreover, current source inverters (CSIs) are considered as good options due to their higher reliability, fault tolerant capabilities, quasi soft switching and using lower capacitor values in comparison with the others. MPC, which is considered as one of the best control methods for power converters, is implemented on this converter. A proper discretization method, an approximation of the parameters, and 2 horizons for calculations of the cost function is used in the MPC controller. In this paper, first, the four operating modes of the converter are demonstrated. Then, the implemented MPC algorithm is described. Simulation results are demonstrated which validates the theoretical calculations and investigations.**

Keywords—Model predictive control, current-source, transformer-less, grid-connected inverter, common-ground

I. Introduction

More than 99% of the installed solar power capacity is allocated to grid-connected systems which shows a significant superiority over stand-alone systems, which use batteries [1],[2]. Compared with stand-alone systems, grid-connected systems are more cost-effective and require less maintenance and reinvestment due to the absence of batteries [3]. This concept together with the cost reduction, technology development, environmental awareness, and the right incentives and regulations has unleashed the power of the sun. Therefore, there has been an increasing interest in grid integration of inverters over the recent years especially because of the increase in using roof-top photovoltaics panels and other renewable energy sources [4].

A transformer is often used to provide galvanic isolation and voltage ratio transformations in PV systems [5]-[6]. However, along with its benefits, not only it increases the weight, size, and cost of the inverter but also reduces the inverter's efficiency and power density [7],[8]. Hence, transformer-less inverters have attracted a lot of research interest and also attention in the residential market [9],[10].

Despite addressing the prevalent problems with the presence of transformers, transformer-less inverters also struggle with some problems [11]. An efficient structure of a transformer-less inverter should tackle the issues including the voltage ratio, the grid voltage amplitude, and power quality [12]. However, the most problematic item in the circuit feasibility of transformer-less PV grid-connected inverters is Medium-frequency

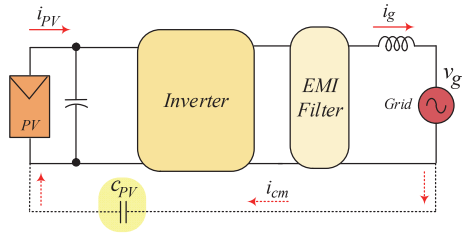

Fig. 1. The general layout of a single-phase transformer-less inverter.

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common-mode current at the inverter switching frequency, which is known as leakage current [13]. As shown in Fig. 1, the parasitic capacitor C_{PV} creates the leakage current i_{cm}, which flows from the negative terminal of the grid to the ground terminal of the PV [14]. It can cause various problems such as injecting harmonics into the grid current, increasing the system losses, decreasing the safety of equipment and personnel, and saturating the core of other involved distributed transformers in the ac grid [15].

According to VDA 0126-1-1 IEEE Standard, 300 mA is the limit of the leakage current [16]. There are various methods of reducing the leakage current three of which are as follows: separating the PV array from the ac side during the freewheeling mode, connecting the grid neutral point to the negative terminal of the PV array directly and clamping the common mode voltage by connection of the neutral point of the grid to the middle point of the two input dc link capacitors. [17].

CSIs are proper choice for grid-connected PV systems since they have the ability to increase input dc voltage that ameliorate using low-voltage PV Systems in grid-connected applications, without any need for extra dc-dc boost converter or transformer [18]. Moreover, they benefit from the inherent current limiting capability, low electromagnetic interference and high reliability [19].

In this paper, the MPC control method is implemented on a non-isolated grid-tied inverter is presented. In this converter, the negative terminal of the PV array connected to the neutral point of the grid, which eliminates the leakage current. In addition, the presented structure has buck-boost ability, which eliminates the need to a dc-dc chopper to work in the voltages of PV below the voltages of the grid. The presented inverter operates as a current source inverter and demands acceptable number of active and passive components, which makes it more efficient and more suitable for further research. In the first step of this paper, the converter is presented and switching states and operating modes are explained. Then, the implemented control system is described in detail. Finally, Simulations results of the converter are demonstrated in order to verify the findings and claims.

II. Investigation of The Topology

Fig. 2 presents the inverter, which includes a power switch with body diode and four four-quadrant switches, one flying inductor and the output filter. The four four-quadrant switches could me any of the three switches shown in fig. 2. The flying inductor L_f is used to boost the input voltage and inject the power of the PV to the grid. The output filter, capacitor C_f, is used to suppress the output harmonics and L_g is the inductor of the grid. During all modes, just two switches are conducted at any moment.

The switching states of the presented converter are shown in table. 1 in which charging and discharging states of the capacitor and inductor are shown by 1 and 0 respectively.

The switching patterns of the power switches are shown in Fig. 3. The inductor's current i_L tracks the reference current i_{ref} via the MPC.

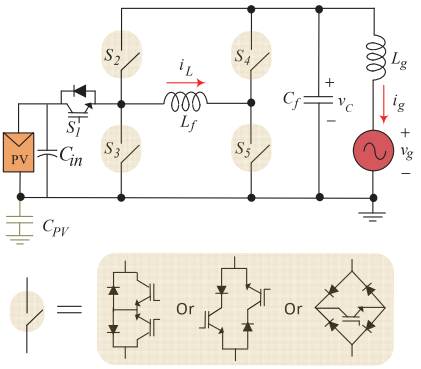

Fig. 2. The presented current-source common-ground inverter.

TABLE I. The switching states of the inverter (1 is for charging state, and 0 is for discharging state of the passive elements).

Modes	Switching States					C_f	L_a
	S_1	S_2	S_3	S_4	S_5		
Mode 1	on	off	off	off	on	0	1
Mode 2	off	on	on	off	off	1	0
Mode 3	on	off	off	off	on	0	1
Mode 4	off	on	off	off	on	1	0

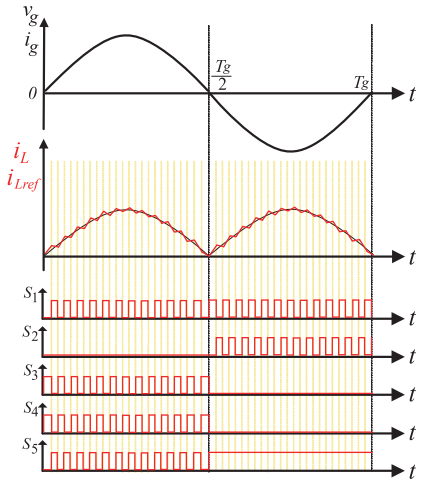

Fig. 3. The waveforms of the grid current, the reference current, and gate signals of the switches.

III. Operating Modes

The converter has four operating modes which are shown in Fig. 4. Two of them, modes 1 and 2, occur only in positive half power cycle repeatedly one after each other. The other two (modes 3 and 4) occur in negative half power cycle. Modes 1 and 3 are similar to each other in which switches S_1 and S_5 are turned on with the difference that the power flows clockwise to

the grid in mode 1 and counterclockwise in mode 3. Like the buck-boost dc-dc converter in both positive and negative half power cycles, first the energy is stored in the inductor via switches S_1 and S_2 and then, the stored energy is injected to the grid via other switches working in the corresponding positive or the negative half power cycle. Eventually, it should be mentioned that as can be seen in Fig. 4, there are always two semiconductors in the conduction path.

A. *Positive half power cycle*

During the positive cycle, modes 1 and 2 occur one after each other. In mode 1, switches 1 and 5 are conducted in order to store the energy of the PV system in the flying inductor. Simultaneously, the power which has been stored in the filter capacitor during the previous mode, is discharged and feeds the grid. In mode 2, the energy which has been stored in the flying inductor in mode 1, flows clockwise and charges the capacitor and it feeds the grid simultaneously.

B. *Negative half power cycle*

Negative cycle includes modes 3 and 4. Similar to mode 1, in mode 3 the inductor La stores energy that comes from the PV panels and it releases this energy in next mode which is mode 4. The filter capacitor C_f is charged in mode 3 via the grid and is discharged in mode 2.

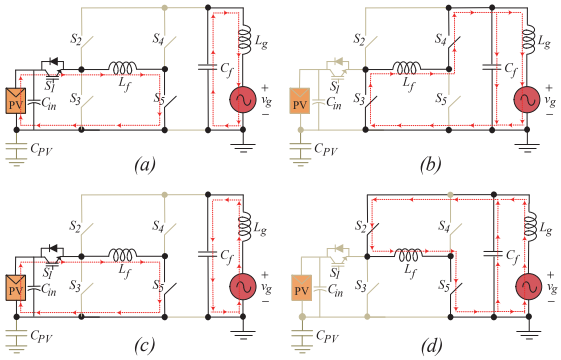

Fig. 4. The operating modes of the presented grid-connected inverter (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4.

IV. The Implemented MPC

MPC is a powerful class of controllers that uses the model of the system for the future behavior prediction and selecting the optimal control actuation [20]. It has notable features, such as straightforward implementation, fast dynamic response, and capable of using nonlinearities. Herein, MPC has been extensively employed in various power electronic applications, especially for power converters feeding nonlinear load conditions [21]. In MPC, based on the model of the system, the future value of the variables can be predicted. By comparing the predicted value and the desired reference value, the control action at the present time is determined [22],[23].

In order to obtain the equations of predicted values, first, we need the equivalent circuits of the converter. Fig. 5(a) shows the equivalent of the converter when switches S_1 and S_5 are on and Fig. 5(b) demonstrates the equivalent when either switches S_3 and S_4 or switches S_2 and S_5 are turns on.

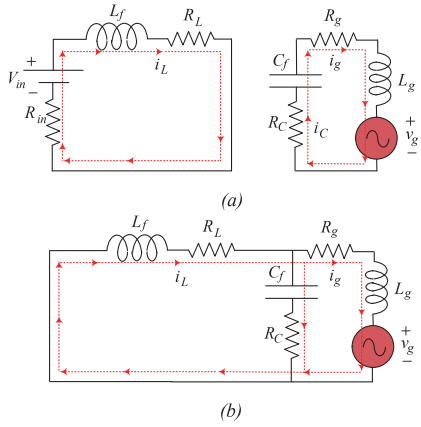

Fig. 5. The equivalent circuits of the inverter, a) when switch S1 is on, b) when switch S1 is off.

By using the Euler method for the equivalent circuit in Fig. 5(a), we obtain equations (1) to (3):

$$L\frac{di_L}{dt}+i_L(R_L+R_{in})=V_{in}, \tag{1}$$

$$L_g\frac{di_g}{dt}+i_g(R_g+R_C)+V_g-V_C=0, \tag{2}$$

$$C\frac{dV_C}{dt}=-i_g. \tag{3}$$

Using the Euler method for the equivalent circuit in Fig. 5(b) results in the following equations:

$$L\frac{di_L}{dt}+R_Li_L+R_CC\frac{dV_C}{dt}+V_C=0, \tag{4}$$

$$L_g\frac{di_g}{dt}+R_gi_g-R_Ci_C+V_g-V_C=0, \tag{5}$$

$$C\frac{dV_C}{dt}=i_L-i_g. \tag{6}$$

To get a discrete-time model it is necessary to use some discretization methods. For first-order systems it is useful, because it is simple, to approximate the derivatives using the Euler forward method, that is:

$$L\frac{di_L}{dt}+R_Li_L+R_CC\frac{dV_C}{dt}+V_C=0. \tag{7}$$

When the order of the system is higher, the discrete-time model obtained using the Euler method is not so good because the error introduced by this method for higher order systems is significant. For these higher order systems, a precise discretization must be used. By using equation (1) for derivatives of V_C, i_L, and i_g, we obtain the equations (8) to (10):

$$\frac{dV_C}{dt} = \frac{V_C[k+1] - V_C[k]}{t_{k+1}}, \quad (8)$$

$$\frac{di_L}{dt} = \frac{i_L[k+1] - i_L[k]}{t_{k+1}}, \quad (9)$$

$$\frac{di_g}{dt} = \frac{i_g[k+1] - i_g[k]}{t_{k+1}}. \quad (10)$$

To get a more precise result, in the calculations, instead of using a value, we use the middle point of that value and the previous one that are shown as blue circle dots in Figs. 6a and 6b.

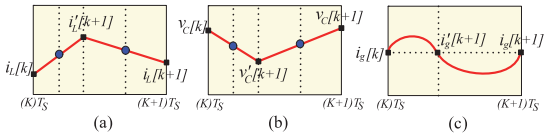

Fig.6. The waveforms of a) the inductor current, b) the capacitor voltage, and c) the grid current, over a period Ts.

Equations (11) to (14), explain this approximation. However, according to equations (15) and (16), since the voltage of the grid inductor is almost zero, its current (i_g) does not change abruptly and using the approximation makes no sense (Fig. 6(c)).

$$V'_C[k+1] \rightarrow \frac{V'_C[k+1] + V_C[k]}{2}, \quad (11)$$

$$V_C[k+1] \rightarrow \frac{V_C[k+1] + V'_C[k+1]}{2}, \quad (12)$$

$$i'_L[k+1] \rightarrow \frac{i'_L[k+1] + i_L[k]}{2}, \quad (13)$$

$$i_L[k+1] \rightarrow \frac{i_L[k+1] + i'_L[k+1]}{2}, \quad (14)$$

$$V_{Lg}[k] \approx V'_{Lg}[k+1] \approx V_{Lg}[k+1] \approx 0, \quad (15)$$

$$i_g[k] \approx i'_g[k+1] \approx i_g[k+1]. \quad (16)$$

The reference voltages of the grid are as follows:

$$V_g[k+1] = V_m \sin(\omega t + \theta), \quad (17)$$

$$V_g[k+2] = V_m \sin(2\omega t + \theta). \quad (18)$$

By using the equations (8) to (14) in equations (1) and (4), we reach the following equations for the inductor's current i_L:

$$i'_L[k+1] = \frac{Li_L[k] + d_{k+1}T_S V_{in}}{L + d_{k+1}T_S(R_L + R_{in})}, \quad (19)$$

$$i_L[k+1] = \frac{Li'_L[k+1] - (1-d_{k+1})T_S(R_g i_g[k] + V_g[k+1])}{L + (1-d_{k+1})T_S(R_L)}. \quad (20)$$

Here, we just control i_L, which is enough to get the desired result. For controlling V_C and i_g, equations similar to (19) and (20) can be written for V_C and i_g.

Fig.7 demonstrates a sample of inductor's current tracking the inductor's reference current. At the time KT_S, there are five options for inductor's current to track the reference current over one period. At the beginning of the second horizon, for each of those five iterations in the first horizon, there are five iterations. Therefore, there are 25 options to reach to end of horizon 2.

The cost function CF_{ij} is the sum of the difference of inductor's current and its reference current over two horizons. In equation (21), i and j refer to the iterations number in horizons 1 and 2 respectively and each of them is a number from 1 to 5.

$$CF_{ij} = \left\| \begin{matrix} i'_L[k+1] - i_{Lref}[k+1] \\ +i_L[k+1] - i_{Lref}[k+1] \end{matrix} \right\|_i + \left\| \begin{matrix} i'_L[k+2] - i_{Lref}[k+2] \\ +i_L[k+2] - i_{Lref}[k+2] \end{matrix} \right\|_j . \quad (21)$$

CF_{min} is the minimum value of CF_{ij}. The duty cycle that corresponds to the CF_{min} will be the value of the modulation signal in the period number k+1. For the next period, horizon 2 in the previous period will be the new horizon 1 and the same strategy will be applied to obtain d_{k+2}.

$$CF_{\min} = \min\left\{CF_{ij}\right\}_{\substack{i=1..5 \\ j=1..5}}. \quad (22)$$

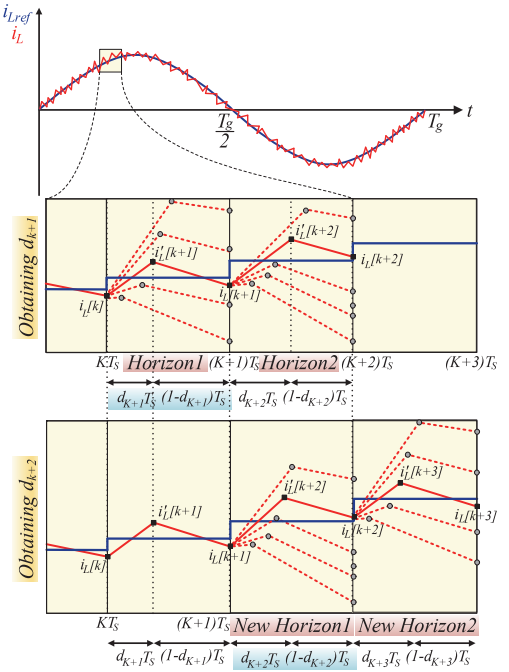

Fig.7. A sample of inductor's current tracking the inductor's reference current.

As shown in Fig. 7, the outputs of the PLL block (ω and V_m) and the current of the inductor L, are given to the predictive controller. Then in the minimization block, cost functions are calculated using the predicted value of the inductor's current and the reference value of the inductor's current. The minimum of the cost functions to produce the modulating signal for Pulse width modulation block, which produces gate signals of the switches.

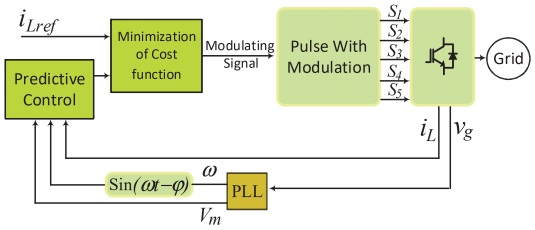

Fig.7. The schematic of the control strategy of the presented converter.

Fig. 8 depicts the flowchart of the MPC controller implemented in the inverter. For i=1 to 5, and j=1 to 5, the cost functions of each horizon are calculated and then the minimum of the 25 obtained cost functions, along with d_{k+1}, which corresponds to the minimum cost function, will be obtained.

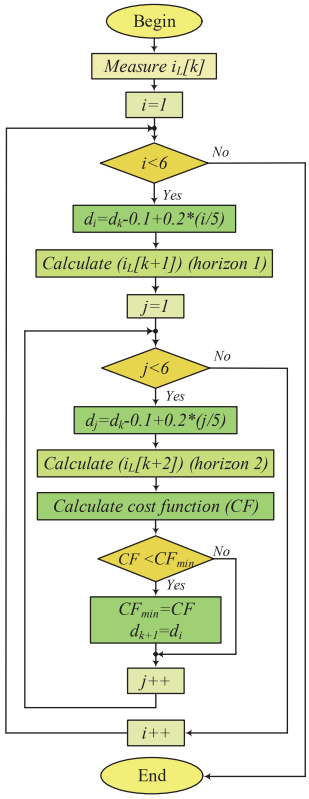

Fig.8. The flowchart of the MPC controller.

V. Simulation Results

The simulation Parameters of the presented converter are declared in Table II. The injected power to the grid equals to 1600 W and the rms value of the grid's voltage is 230 V.

In Fig. 9(a), the waveform of the grid current is shown in red, and the voltage of the grid is demonstrated in blue. The scale of the grid voltage is 1/20. It is seen that the voltage and current of the grid are in phase. In addition, the whole injected power to the grid is active power and there is no injected reactive power to the grid. The voltage of the output filter capacitor is synchronous with the grid as shown in Fig. 9(b). The waveform of the flying

parameter	value
Rated Power, P	1600 W
Input Voltage, V_{in}	200 V
Grid voltage (Peak Value), V_m	320 V
Flying inductor, L_f	1.6 mH
Grid inductor, L_g	0. 35 mH
Filtering Capacitor, C_f	2 μF
Resistances of PV, flying inductor, filtering capacitor, and grid, R_{in}, R_L, R_C, R_g	0.1 Ω
Fundamental frequency, f_g	50 Hz
Switching frequency, f_s	62.5 kHz

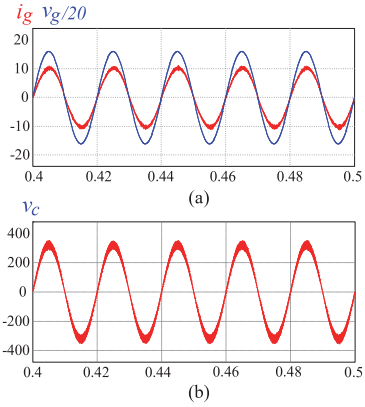

Fig.9. The waveforms of (a) grid voltage and current (b) capacitor voltage.

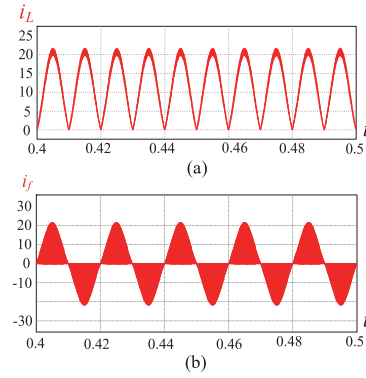

Fig.10. The waveforms of (a) the current of the flying inductor (b) the current of the output filter.

inductor's current is shown in Fig. 10(c). It is shown that the MPC controller system has been designed in the way that the current of the flying inductor completely tracks its reference waveform. The peak of its value is 27 A. The filter's input current is demonstrated in Fig. 10(d). The peak of this current is 27 A in the positive half cycle and -27 A in the negative half cycle.

VI. Conclusion

An MPC controller has been implemented on a current source inverter, which benefits from common-grounding feature. This continuous-control-set MPC has been used to make a smooth injected current to the grid. A precise discretization method has been used for derivatives of the parameters. In addition, an approximation of these parameters is implemented in equations to make the prediction more accurate. Two horizons with 5 iterations in each, has been used for the MPC. The 25 iterations have been enough to achieve the desired result and suitable for calculation by the microcontroller. Using a simple but effective cost function, the algorithm shows a good reference tracking and a robust behavior which has been demonstrated in the simulation results.

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